



# STIC EIC 2100 110094 Search Request Form

Today's Date: 12/9/03

What date would you like to use to limit the search?

Priority Date: 11/29/00

Other:

Name MARK CONNOLLY

AU 2185 Examiner # 79656

Room # 2B08 Phone 305-7849

Serial # 09/733382

Format for Search Results (Circle One):

PAPER DISK EMAIL

Where have you searched so far?

USP DWPI EPO JPO ACM IBM TDB

IEEE INSPEC SPI Other

Is this a "Fast & Focused" Search Request? (Circle One) YES NO

A "Fast & Focused" Search is completed in 2-3 hours (maximum). The search must be on a very specific topic and meet certain criteria. The criteria are posted in EIC2100 and on the EIC2100 NPL Web Page at <http://ptoweb/patents/stic/stic-tc2100.htm>.

What is the topic, novelty, motivation, utility, or other specific details defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, definitions, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract, background, brief summary, pertinent claims and any citations of relevant art you have found.

AN INSTRUCTION WHICH CAN BE USED ACROSS MULTIPLE PLATFORMS  
(i.e. IBM COMPATIBLE, MAC, UNIX) WHICH DEFINES A LOCATION OR ADDRESS  
OF A PARTICULAR DATA ELEMENT ALONG WITH THE LENGTH OR SIZE OF  
THE DATA ELEMENT

STIC Searcher Tereese Esterheld

Phone 308-7795

Date picked up 12/9/03 3:00pm

Date Completed 12/10/03 9:30am



Set	Items	Description
S1	2991814	INSTRUCTION? OR STATEMENT? OR OPERATION? OR FUNCTION? OR EXECUTION? OR COMMAND?
S2	2287358	DEFINE? OR DEFINING OR SPECIF? OR DESCRIB? OR STIPULAT? OR DESIGNAT?
S3	732764	ADDRESS? OR LOCATION OR LINK? ? OR URL OR URLS OR (UNIFORM OR UNIVERSAL) ()RESOURCE()LOCATOR? OR NAMESPACE OR DOMAIN
S4	51565	DATA (2N) (ELEMENT? OR VALUE? OR ATTRIBUTE? OR TRAIT? OR FEATURE?)
S5	3628168	LENGTH OR SIZE? OR SIZING OR CAPACITY? OR LIMIT? OR EXTENT OR BOUNDAR? OR THRESHOLD OR STREAM? OR BLOCK?
S6	3090	(MULTIPLE OR MANY OR PLURAL? OR NUMEROUS OR SEVERAL OR DUPLICAT) (2N) (PLATFORM? OR (COMPUTER? OR OPERATING) ()SYSTEM?)
S7	1234	S1 AND S6
S8	640962	S2 AND (S3 OR S4 OR S5)
S9	155321	S2 ( 5N) (S3 OR S4 OR S5)
S10	41	S7 AND S8 AND S9
S11	36	S10 AND IC=G06F?

File 347:JAPIO Oct 1976-2003/Aug(Updated 031202)

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File 350:Derwent WPIX 1963-2003/UD,UM &UP=200379

(c) 2003 Thomson Derwent

11/5/4 (Item 4 from file: 347)  
DIALOG(R) File 347:JAPIO  
(c) 2003 JPO & JAPIO. All rts. reserv.

04551024 \*\*Image available\*\*  
WRITING METHOD FOR FLASH MEMORY

PUB. NO.: 06-222924 [JP 6222924 A]  
PUBLISHED: August 12, 1994 (19940812)  
INVENTOR(s): HARA KENJI  
APPLICANT(s): YASKAWA ELECTRIC CORP [000662] (A Japanese Company or Corporation), JP (Japan)  
APPL. NO.: 05-011789 [JP 9311789]  
FILED: January 27, 1993 (19930127)  
INTL CLASS: [5] G06F-009/445  
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)  
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessors)  
JOURNAL: Section: P, Section No. 1826, Vol. 18, No. 600, Pg. 152, November 15, 1994 (19941115)

#### ABSTRACT

PURPOSE: To write a program in a flash memory without always mounting any ROM different from the flash memory to a computer system.  
CONSTITUTION: This method uses the **computer system** provided with **plural** resistors R(sub 19)-R(sub 0) for pull-down or pull-up for preparing one word of a jump **instruction** for each data line of a data bus 7 when each data line of the data bus 7 is in a floating state and a flash memory 2 to which the **address** of the jump destination **designated** by the jump **instruction** fixed by the resistors R(sub 19)-R(sub 0) is allocated. When the system program has not been written yet, a freely attachable and detachable ROM, to which the restart **address** of a CPU 1 is allocated, is mounted on the computer system, when the boot program of the ROM is executed, the system program is written in the flash memory 2 corresponding to any computer different from the computer system, and the ROM is detached later.

11/5/5 (Item 5 from file: 347)  
DIALOG(R) File 347:JAPIO  
(c) 2003 JPO & JAPIO. All rts. reserv.

04350423 \*\*Image available\*\*  
**COMMAND** TRANSFER SYSTEM FOR NETWORK SYSTEM

PUB. NO.: 05-342123 [JP 5342123 A]  
PUBLISHED: December 24, 1993 (19931224)  
INVENTOR(s): OOHATA YOSHIYORI  
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)  
APPL. NO.: 04-149030 [JP 92149030]  
FILED: June 09, 1992 (19920609)  
INTL CLASS: [5] G06F-013/00 ; G06F-015/16  
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 45.4 (INFORMATION PROCESSING -- Computer Applications)  
JOURNAL: Section: P, Section No. 1718, Vol. 18, No. 181, Pg. 132, March 28, 1994 (19940328)

#### ABSTRACT

PURPOSE: To transfer a **command** to a remote system without allowing a user to be aware of a difference of the kind of a machine to be connected, in the network system.  
CONSTITUTION: The network system consists of **plural computer systems**. A **command** analysis processing part 3 in each computer system executes an analysis of a **command** name and its parameter. A system determination processing part 4 determines a system for executing a **command** by the **location** of resources **designated** by the parameter of the **command**, an

operating state of the system, a supporting state of the command and the performance of the system. A remote command request processing part 10 converts the command to a command format of the system of a transfer destination, transfers the command to a remote system, edits its result and outputs it to a terminal.

11/5/6 (Item 6 from file: 347)  
DIALOG(R) File 347:JAPIO  
(c) 2003 JPO & JAPIO. All rts. reserv.

03982656 \*\*Image available\*\*  
CHANNEL STATE READ SYSTEM

PUB. NO.: 04-347756 [JP 4347756 A]  
PUBLISHED: December 02, 1992 (19921202)  
INVENTOR(s): MIHASHI SHINICHI  
MORI SHIGERU  
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP  
(Japan)  
HITACHI COMPUT ENG CORP LTD [472484] (A Japanese Company or Corporation), JP (Japan)  
APPL. NO.: 03-119895 [JP 91119895]  
FILED: May 24, 1991 (19910524)  
INTL CLASS: [5] G06F-013/12 ; G06F-013/14  
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)  
JOURNAL: Section: P, Section No. 1525, Vol. 17, No. 207, Pg. 74, April 22, 1993 (19930422)

#### ABSTRACT

PURPOSE: To process a channel state storage instruction which is to store state information on a channel connected to an input/output processor on a main storage device in a computer system.

CONSTITUTION: In the computer system in which plural instruction processors 1 are connected to the input/output processor 3 having plural channels 4 through a system controller 2 and which has the main storage device 5 shared by the respective instruction processors 1 and the input/output processor 3, a private area 20 shared by the systems is provided on the storage device 5 to which the instruction processors 1 and the input/output processor 3 can access, and the input/output processor 3 stores information on the channel state in the private area 20 at every prescribed time. For executing the channel state storage instruction of the instruction processor 1, information on the channel state stored in the private area 20 is read from the input/output processor 3 and it is storage-processed in the designated address of the main storage device 5.

11/5/7 (Item 7 from file: 347)  
DIALOG(R) File 347:JAPIO  
(c) 2003 JPO & JAPIO. All rts. reserv.

02007821 \*\*Image available\*\*  
RISING SYSTEM FOR OPERATING SYSTEM

PUB. NO.: 61-221921 [JP 61221921 A]  
PUBLISHED: October 02, 1986 (19861002)  
INVENTOR(s): MORIYA KEIZO  
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP  
(Japan)  
APPL. NO.: 60-064890 [JP 8564890]  
FILED: March 28, 1985 (19850328)  
INTL CLASS: [4] G06F-001/00  
JAPIO CLASS: 45.9 (INFORMATION PROCESSING -- Other)  
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessors)

ABSTRACT

PURPOSE: To enable a personal computer operator to select an operating system OS which is actuated by a personal computer with no complicated **operation**, by using a system file storing plural systems OS to attain the rise of a personal computer system.

CONSTITUTION: A system file FD14 stores **plural operating systems** OS, and a slide switch 1 is set to send the selection signal to a CPU circuit 3 of a personal computer for selection of an OS. The power supply of the personal computer is applied after the switch 1 is set. Then a floppy disk FD is loaded to an FD device. A program **address** for rise of a personal computer system corresponding to an OS type set previously by the switch 1 is selected by an **address** switching circuit 5. Then the **designated** OS is read out of a BIOS storing circuit 6 by said program **address**. The circuit 3 rises the system with the **designated** OS and executes a program.

11/5/9 (Item 2 from file: 350)  
DIALOG(R) File 350:Derwent WPIX  
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015625597 \*\*Image available\*\*  
WPI Acc No: 2003-687768/200365  
Related WPI Acc No: 2000-431665; 2003-455934  
XRAM Acc No: C03-188546  
XRPX Acc No: N03-549384

**Computer readable medium, useful for characterizing organic or inorganic materials, contains software comprising instructions for calculating an arithmetic value corresponding to material property and storing, e.g. the calculated value**

Patent Assignee: SYMYX TECHNOLOGIES INC (SYMY-N)  
Inventor: BENNETT J; MANSKY P  
Number of Countries: 001 Number of Patents: 001  
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030101006	A1	20030529	US 98210086	A	19981211	200365 B
			US 98210428	A	19981211	
			US 98210485	A	19981211	
			US 99458398	A	19991210	
			US 2002315519	A	20021210	

Priority Applications (No Type Date): US 99458398 A 19991210; US 98210086 A 19981211; US 98210428 A 19981211; US 98210485 A 19981211; US 2002315519 A 20021210

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 20030101006	A1	90	G06F-019/00	CIP of application US 98210086 CIP of application US 98210428 CIP of application US 98210485 Cont of application US 99458398 CIP of patent US 6438497 CIP of patent US 6477479 Cont of patent US 6535824

Abstract (Basic): US 20030101006 A1

NOVELTY - A computer readable medium contains:

- (1) software comprising **instructions** for computing, selecting and setting test equipment operating parameters;
- (2) **instructions** for calculating an arithmetic value corresponding to material property; and
- (3) **instructions** for monitoring and storing the calculated arithmetic **value**, raw **data**, and each **specific** output for each signal processed.

DETAILED DESCRIPTION - A computer readable medium contains software

for the control of **operation** of an apparatus for characterizing material properties for samples. The software comprises:

- (1) **instructions** for selecting a sensor(s) for measurement;
- (2) **instructions** for computing, selecting and setting the test equipment operating parameters;
- (3) **instructions** for initiating a data gathering sequence;
- (4) **instructions** for sending, receiving and monitoring signals sent to and received from sensor(s);
- (5) **instructions** for processing signals received from the sensor(s);
- (6) **instructions** for calculating an arithmetic value corresponding to material property using **specific** output generated for signal processed; and
- (7) **instructions** for monitoring and storing the calculated arithmetic value, raw data, and each **specific** output for each signal processed.

USE - The computer readable medium is used for characterizing organic or inorganic materials.

ADVANTAGE - The apparatus is capable of measuring properties of many material samples quickly and simultaneously and connecting to a flexible electronic **platform** to allow **many** different material properties to be measured with minimal modification of the apparatus.

DESCRIPTION OF DRAWING(S) - The drawing shows a structure of the computer readable medium.

Sensor array (10)

Mounting plate (17)

Standard combinatorial chemistry wells (84)

pp; 90 DwgNo 8/28

Title Terms: COMPUTER; READ; MEDIUM; USEFUL; CHARACTERISTIC; ORGANIC; INORGANIC; MATERIAL; CONTAIN; SOFTWARE; COMPRISE; **INSTRUCTION**; CALCULATE; ARITHMETIC; VALUE; CORRESPOND; MATERIAL; PROPERTIES; STORAGE; CALCULATE; VALUE

Derwent Class: B04; J04; T01

International Patent Class (Main): **G06F-019/00**

File Segment: CPI; EPI

11/5/12 (Item 5 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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012954294 \*\*Image available\*\*

WPI Acc No: 2000-126144/200011

XRPX Acc No: N00-095096

**Single instruction seizing of control of a program execution flow in a multiple-processor computing system**

Patent Assignee: BMC SOFTWARE INC (BMCS-N)

Inventor: SHEARER B L

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6014740	A	20000111	US 97834025	A	19970411	200011 B

Priority Applications (No Type Date): US 97834025 A 19970411

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 6014740	A	13	G06F-009/30	

Abstract (Basic): US 6014740 A

NOVELTY - A method of dynamically altering a computer program in memory utilizes a branching **instruction** causing the processor system to jump, not to a **specific address**, but to an **address** that is a **specified** number of bytes in memory away from the current **instruction**'s **address**. Relative branching **instructions** are supported in HP UNIX systems and in most modern RISC processor-based systems. A predetermined segment of code is set up in memory to handle a hooking **operation** and is executed after the processor system executes the

relative branching **instructions** , which is carried out by patching the software to insert a single relative-branch **instruction** .

DETAILED DESCRIPTION - AN INDEPENDENT CLAIM is included for a computer-readable program storage device.

USE - Modifying software controlling **operation** of a **multiple** -processor **computer system** .

DESCRIPTION OF DRAWING(S) - The drawing is a simplified flow chart of the **operations** performed in executing a method according to the invention.

pp; 13 DwgNo 5/6

Title Terms: SINGLE; **INSTRUCTION** ; SEIZE; CONTROL; PROGRAM; EXECUTE; FLOW; MULTIPLE; PROCESSOR; COMPUTATION; SYSTEM

Derwent Class: T01

International Patent Class (Main): **G06F-009/30**

International Patent Class (Additional): **G06F-009/38 ; G06F-009/44**

File Segment: EPI

**11/5/13 (Item 6 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

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012673416 \*\*Image available\*\*

WPI Acc No: 1999-479523/199940

XRPX Acc No: N99-356986

**Data management system providing client access**

Patent Assignee: MERRILL LYNCH & CO INC (MERR-N)

Inventor: FORD C; LAKSHMANAN M; SCALF R S

Number of Countries: 075 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9940519	A1	19990812	WO 99US1900	A	19990128	199940 B
AU 9925671	A	19990823	AU 9925671	A	19990128	200005
US 6047324	A	20000404	US 9819233	A	19980205	200024
US 6374299	B1	20020416	US 9819233	A	19980205	200232
			US 2000491815	A	20000126	

Priority Applications (No Type Date): US 9819233 A 19980205; US 2000491815 A 20000126

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

WO 9940519 A1 E 36 G06F-015/16

Designated States (National): AL AM AU BA BB BG BR CA CN CU CZ EE GE HR HU ID IL IN IS JP KP KR LC LK LR LT LV MG MK MN MX NO NZ PL RO SG SI SK SL TR TT UA UZ VN YU

Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW

AU 9925671 A Based on patent WO 9940519

US 6047324 A G06F-015/10

US 6374299 B1 G06F-015/10 Cont of application US 9819233

Cont of patent US 6047324

Abstract (Basic): WO 9940519 A1

NOVELTY - The system is a program controlled **computer system** comprised of **multiple** client nodes interconnected in a network to central servers and linked to a variety of select services for information retrieval and provision in accordance with program logic.

DETAILED DESCRIPTION - The data processing architecture provides a common grouping of code that supports a diverse set of services and allows seamless access to these services by clients. The architecture is supported by several interrelated components. A framework executable (250) provides the common code structures and the services **specific functionality** is provided by conforming dynamic **link** library routines (DLLs) **specific** to that service. System **operation** is enhanced by a router (220) that allocates service loading in accordance with demand and availability.

USE - The system is used to manage the access and communication

across a number of interconnected computers including network servers and mainframes, with data and application access via a public network such as Internet.

ADVANTAGE - Because a common code framework characterizes much of the complex communication coding, developers seeking to implement new services can concentrate on creating service **functionality** and rely on the framework for this communication and navigation support.

DESCRIPTION OF DRAWING(S) - The figure provides an overview of the system.

pp; 36 DwgNo 3A/9

Title Terms: DATA; MANAGEMENT; SYSTEM; CLIENT; ACCESS

Derwent Class: T01; W01

International Patent Class (Main): G06F-015/10 ; G06F-015/16

File Segment: EPI

11/5/14 (Item 7 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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010704081 \*\*Image available\*\*

WPI Acc No: 1996-201036/199620

Related WPI Acc No: 1995-132820; 1996-268192; 1996-476664; 1997-502662

XRPX Acc No: N96-168653

**File linking between emulation and host for emulation users - has host processor including application providing emulation and emulator monitor with security checking for host and emulation**

Patent Assignee: BULL HN INFORMATION SYSTEMS INC (HONE )

Inventor: BIANCHI R S; HIRSCH T S; PERRY R B

Number of Countries: 017 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9610224	A2	19960404	WO 95US12354	A	19950912	199620 B
WO 9610224	A3	19960509	WO 95US12354	A	19950912	199630
US 5572711	A	19961105	US 93128456	A	19930928	199650
			US 94311646	A	19940923	
EP 803101	A1	19971029	EP 95935148	A	19950912	199748
			WO 95US12354	A	19950912	
EP 803101	B1	20030618	EP 95935148	A	19950912	200341
			WO 95US12354	A	19950912	
DE 69531112	E	20030724	DE 631112	A	19950912	200356
			EP 95935148	A	19950912	
			WO 95US12354	A	19950912	

Priority Applications (No Type Date): US 94311646 A 19940923; US 93128456 A 19930928

Cited Patents: US 4611298; US 4621321; US 4825354; US 4918653; US 4984272; US 5204961; US 5361359

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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WO 9610224	A2	E	91	G06F-000/00	
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Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE

WO 9610224	A3			G06F-000/00	
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US 5572711	A		19	G06F-003/00	CIP of application US 93128456
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EP 803101	A1	E		G06F-017/30	Based on patent WO 9610224
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Designated States (Regional): DE FR GB IT

EP 803101	B1	E		G06F-017/30	Based on patent WO 9610224
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Designated States (Regional): DE FR GB IT

DE 69531112	E			G06F-017/30	Based on patent EP 803101
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Based on patent WO 9610224

Abstract (Basic): WO 9610224 A

The host data processing system has a variety of input-output devices and operates under an extended UNIX operating system. The host includes an emulator that runs as an application process to execute user emulated system applications.



The emulator (28) has a number of emulated system executive services operating in shared memory. An interpreter, an emulator monitor call unit (EMCU) (73) and a number of server facilities operate in the host memory. The emulator and file manager are extended to allow creation and access to linked files within both the host and the emulation environment. Security facilities are extended to maintain the integrity of both systems.

ADVANTAGE - Allows efficient access and control of host files for application program operating in an emulation environment.

Dwg.1a/2

Title Terms: FILE; **LINK** ; EMULATION; HOST; EMULATION; USER; HOST; PROCESSOR; APPLY; EMULATION; EMULATION; MONITOR; SECURE; CHECK; HOST; EMULATION

Derwent Class: T01

International Patent Class (Main): **G06F-000/00** ; **G06F-003/00** ;

**G06F-017/30**

International Patent Class (Additional): **G06F-009/455** ; H04L-009/00

File Segment: EPI

11/5/15 (Item 8 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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009967203 \*\*Image available\*\*

WPI Acc No: 1994-234916/199428

XRPX Acc No: N94-185651

**Object-oriented framework for object operating system - translates input syntax into semantic operations for object that supports select, peek, move, auto-scroll and drag/drop or copy**

Patent Assignee: TALIGENT INC (TALI-N); OBJECT TECHNOLOGY LICENSING CORP (OBJE-N); OTLC (OTLC-N); OBJECT LICENSING LICENSING CORP (OBJE-N)

Inventor: GOLDSMITH D B; HENINGER A G; MOELLER C P; ORTON D L; HENNINGER A G

Number of Countries: 047 Number of Patents: 014

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9415286	A1	19940707	WO 93US12192	A	19931214	199428	B
AU 9458278	A	19940719	AU 9458278	A	19931214	199439	
EP 664025	A1	19950726	WO 93US12192	A	19931214	199534	
			EP 94904086	A	19931214		
JP 8505721	W	19960618	WO 93US12192	A	19931214	199648	
			JP 94515273	A	19931214		
CN 1091536	A	19940831	CN 93112880	A	19931223	199715	
EP 664025	B1	19970423	WO 93US12192	A	19931214	199721	
			EP 94904086	A	19931214		
DE 69310187	E	19970528	DE 610187	A	19931214	199727	
			WO 93US12192	A	19931214		
			EP 94904086	A	19931214		
US 5717877	A	19980210	US 92996171	A	19921223	199813	
			US 95482314	A	19950606		
US 6146027	A	20001114	US 92996171	A	19921223	200060	
			US 95482314	A	19950606		
			US 97898768	A	19970723		
US 6327627	B1	20011204	US 92996171	A	19921223	200203	
			US 95482314	A	19950606		
			US 97898768	A	19970723		
			US 99329578	A	19990610		
CA 2145679	C	20021022	CA 2145679	A	19931214	200279	
			WO 93US12192	A	19931214		
JP 2002278667	A	20020927	JP 94515273	A	19931214	200279	
			JP 20029270	A	19931214		
JP 2002278668	A	20020927	JP 94515273	A	19931214	200279	
			JP 20029272	A	19931214		
JP 2002297386	A	20021011	JP 94515273	A	19931214	200281	
			JP 20029271	A	19931214		

Priority Applications (No Type Date): US 92996171 A 19921223; US 95482314 A

19950606; US 97898768 19970723; US 99329578 A 199906

Cited Patents: 01Jnl.Ref

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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WO 9415286	A1	E	64	G06F-009/44	
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Designated States (National): AT AU BB BG BR BY CA CH CZ DE DK ES FI GB

HU JP KP KR KZ LK LU LV MG MN MW NL NO NZ PL PT RO RU SD SE SK UA UZ VN

Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL

OA PT SE

AU 9458278	A			G06F-009/44	Based on patent WO 9415286
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EP 664025	A1	E	64	G06F-009/44	Based on patent WO 9415286
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Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LU MC

NL PT SE

JP 8505721	W		86	G06F-009/44	Based on patent WO 9415286
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CN 1091536	A			G06F-015/00	
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EP 664025	B1	E	46	G06F-009/44	Based on patent WO 9415286
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Designated States (Regional): DE FR GB

DE 69310187	E			G06F-009/44	Based on patent EP 664025
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Based on patent WO 9415286

US 5717877	A		33	G06F-015/00	Cont of application US 92996171
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US 6146027	A			G06F-009/44	Cont of application US 92996171
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Div ex application US 95482314

Div ex patent US 5717877

US 6327627	B1			G06F-015/00	Cont of application US 92996171
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Div ex application US 95482314

Cont of application US 97898768

Div ex patent US 5717877

CA 2145679	C	E		G06F-009/44	Based on patent WO 9415286
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JP 2002278667	A		31	G06F-003/00	Div ex application JP 94515273
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JP 2002278668	A		31	G06F-003/00	Div ex application JP 94515273
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JP 2002297386	A		31	G06F-009/44	Div ex application JP 94515273
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Abstract (Basic): WO 9415286 A

The system provides an object oriented framework using an operating system to process applications, framework processing to standardise applications residing in the operating system including object oriented drivers and a kernel that is object oriented.

A mouse button depressing determines the logic for an option key to enter drag mode using the selected object as the target of the **operation** , or if the option key was not depressed, the system enters selection mode. If the mouse button is held down then alternative logic is followed and the system determines whether the mouse has been moved past a certain **threshold** called the move **threshold** in the window, outside the window, or on the border.

USE - Provides check-box control activation, update, dialog box, colour controller and radio button. Object-oriented application interface using system's graphical user interface with mouse.

Dwg.1/21

Title Terms: OBJECT; ORIENT; FRAMEWORK; OBJECT; OPERATE; SYSTEM;

TRANSLATION; INPUT; SYNTAX; OPERATE; OBJECT; SUPPORT; SELECT; MOVE; AUTO;

SCROLL; DRAG; DROP; COPY

Derwent Class: T01

International Patent Class (Main): G06F-003/00 ; G06F-009/44 ;

G06F-015/00

International Patent Class (Additional): G06F-009/46

File Segment: EPI

11/5/16 (Item 9 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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009942884 \*\*Image available\*\*

WPI Acc No: 1994-210597/199426

Related WPI Acc No: 1990-093063

XRPX Acc No: N94-165850

Parallel computer system using SIMD method - has controller and control

groups with processors used as address control unit with connected scheduling circuits receiving and managing event signal address of data to be processed and transmitted from adjacent group

Patent Assignee: FUJITSU LTD (FUJIT )

Inventor: KAWAMURA K; MIWATARI H; SHIBUYA T; SHINDO T; UMEDA M

Number of Countries: 004 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 605401	A2	19940706	EP 89309445	A	19890918	199426 B
			EP 94104303	A	19890918	
EP 360527	B1	19950104	EP 89309445	A	19890918	199506
EP 605401	A3	19940928	EP 94104303	A	19890918	199533
EP 605401	B1	19980422	EP 89309445	A	19890918	199820
			EP 94104303	A	19890918	
US 36954	E	20001114	US 89409613	A	19890919	200060
			US 95503595	A	19950719	

Priority Applications (No Type Date): JP 88234546 A 19880919; JP 88234545 A 19880919

Cited Patents: 01Jnl.Ref; EP 131658; EP 236762; US 4304002; US 4574345; US 4621339; No-SR.Pub; EP 20202; EP 262750; US 4644496; WO 8804076

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 605401	A2	E	28	G06F-015/80	Related to application EP 89309445
					Designated States (Regional): DE FR GB
EP 360527	B1	E	16	G06F-015/80	
					Designated States (Regional): DE FR GB
EP 605401	A3			G06F-015/80	Related to patent EP 360527
EP 605401	B1	E	28	G06F-015/80	Div ex application EP 89309445
					Div ex patent EP 360527
					Designated States (Regional): GB
US 36954	E			G06F-015/00	Reissue of patent US 5230057

Abstract (Basic): EP 605401 A

The **computer system** comprises **several** control groups (G1 to G4) containing several processors (14) used as an **address** control unit. Several schedulers, one for each group are connected to the controller (10), and receive and manage an event signal **designating** an **address** signal for data to be processed and transmitted from an adjacent control group.

Several real **address** generators (120), one for each control group, are connected between the controller, the scheduler (110) and the control group to generate an **address** signal for the data to be processed by a processor belonging to the control group based on the base **address** determined by the event signal to be managed by the scheduler and an **address** signal from the controller.

ADVANTAGE - Can control all processor elements so as to uniformly and effectively distribute the processor elements as load.

Dwg.4/23

Title Terms: PARALLEL; COMPUTER; SYSTEM; SIMD; METHOD; CONTROL; CONTROL; GROUP; PROCESSOR; **ADDRESS** ; CONTROL; UNIT; CONNECT; SCHEDULE; CIRCUIT; RECEIVE; MANAGE; EVENT; SIGNAL; **ADDRESS** ; DATA; PROCESS; TRANSMIT; ADJACENT; GROUP

Derwent Class: T01; U11

International Patent Class (Main): G06F-015/00 ; G06F-015/80

File Segment: EPI

11/5/17 (Item 10 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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009805833 \*\*Image available\*\*

WPI Acc No: 1994-085688/199411

Related WPI Acc No: 1996-241341

XRPX Acc No: N94-067073

Communication between processes between computer systems connected via

network - storing information related to address of data reception  
area in sender node then accessing virtual data transmission area by data  
sender process

Patent Assignee: HITACHI LTD (HITA )

Inventor: CHIBA H; IWASAKI M; SONODA K; UTSUNOMIYA N; YAMAYUCHI M;  
YOSHIZAWA S; YAMAUCHI M

Number of Countries: 003 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
GB 2271006	A	19940330	GB 9319816	A	19930924	199411 B
GB 2271006	B	19961030	GB 9319816	A	19930924	199647
US 5659777	A	19970819	US 93126088	A	19930923	199739
US 5867656	A	19990202	US 93126088	A	19930923	199912
			US 96759890	A	19961203	

JP 3003418 B2 20000131 JP 92256155 A 19920925 200010

Priority Applications (No Type Date): JP 92256155 A 19920925

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2271006	A		97	G06F-013/38	
JP 3003418	B2	33		G06F-015/177	Previous Publ. patent JP 6110845
GB 2271006	B	1		G06F-013/38	
US 5659777	A	39		G06F-013/38	
US 5867656	A			G06F-013/38	Cont of application US 93126088 Cont of patent US 5659777

Abstract (Basic): GB 2271006 A

In computer networking, transmission and reception buffers (103,104,109-112) of sender and receiver process are prepared as resident areas in main storage. A receiver node (122) notifies, prior to initiation of communication, a physical address of, and access right code of, a data reception area of the node to a sender node (120).

In the sender node, the notified physical address and access right code are added to transmission data. Double buffering (108,110,112) is employed to prevent overwriting of a data reception area already in use. The respective nodes achieve partial synchronisation with adjacent nodes in a chain, thereby automatically establishing synchronisation between all nodes,

USE/ADVANTAGE - For implementation of low overhead high speed communication function necessary for parallel processing etc. Provision for high speed image transfer and parallel arithmetic processing.

Dwg.5/27

Title Terms: COMMUNICATE; PROCESS; COMPUTER; SYSTEM; CONNECT; NETWORK; STORAGE; INFORMATION; RELATED; ADDRESS; REAL; DATA; RECEPTION; AREA; SEND; NODE; ACCESS; VIRTUAL; DATA; TRANSMISSION; AREA; DATA; SEND; PROCESS

Derwent Class: T01

International Patent Class (Main): G06F-013/38 ; G06F-015/177

International Patent Class (Additional): G06F-013/00 ; G06F-015/16 ;

G06F-015/17

File Segment: EPI

11/5/18 (Item 11 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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009721440 \*\*Image available\*\*

WPI Acc No: 1994-001290/199401

XRPX Acc No: N94-001005

Personal computer for modular BIOS device support layer - has microprocessor, non-volatile RAM storing operating system microcode, volatile memory with operating system portion used by microcode, and DASD storing second microcode with several modules

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC )

Inventor: BEALKOWSKI R; BLACKLEDGE J W; BLASCHKE D E; BOLT M; GEISLER D R;

HILLIS R G; SCHROEDER J; TURNER M R; BOLT M M  
Number of Countries: 006 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 576126	A2	19931229	EP 93303472	A	19930504	199401 B
BR 9302438	A	19940216	BR 932438	A	19930622	199410
EP 576126	A3	19940112	EP 93303472	A	19930504	199516
US 5446898	A	19950829	US 92902134	A	19920622	199540
US 5481709	A	19960102	US 92902330	A	19920622	199607
US 5495611	A	19960227	US 92902311	A	19920622	199614
JP 2986306	B2	19991206	JP 93135547	A	19930607	200003

Priority Applications (No Type Date): US 92902330 A 19920622; US 92902134 A 19920622; US 92902311 A 19920622

Cited Patents: Jnl.Ref; EP 100140; EP 358292; EP 419004

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 576126	A2	E	22	G06F-009/445	
Designated States (Regional): DE FR GB					
JP 2986306	B2		20	G06F-009/24	Previous Publ. patent JP 6149562
US 5446898	A		25	G06F-009/44	
US 5481709	A		25	G06F-009/44	
US 5495611	A		24	G06F-009/00	
BR 9302438	A			G06F-013/00	
EP 576126	A3			G06F-009/445	

Abstract (Basic): EP 576126 A

The personal computer system includes a microprocessor and a non-volatile memory both electrically coupled to the data bus. A volatile memory and a DASD are both electrically responsive to the data bus. A memory controller is electrically coupled to the processor, and the volatile and non-volatile memories.

The non-volatile memory stores a first portion of the operating system microcode and the volatile memory includes a volatile operating system portion for use by the microcode. The memory controller regulates communications between the memories and the high-speed microprocessor. The DASD stores a second portion of **operating system** microcode having **several** modules which are selectively accessed by the microprocessor as needed.

USE/ADVANTAGE - for selectively configuring firmware. Optimises use of RAM. Allows modular ABIOS.

Dwg.7/12

Title Terms: PERSON; COMPUTER; MODULE; DEVICE; SUPPORT; LAYER;  
MICROPROCESSOR; NON; VOLATILE; RAM; STORAGE; OPERATE; SYSTEM; VOLATILE;  
MEMORY; OPERATE; SYSTEM; PORTION; DASD; STORAGE; SECOND; MODULE  
Index Terms/Additional Words: DATA; BUS

Derwent Class: T01

International Patent Class (Main): G06F-009/00 ; G06F-009/24 ;  
G06F-009/44 ; G06F-009/445 ; G06F-013/00

File Segment: EPI

11/5/19 (Item 12 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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009676814 \*\*Image available\*\*

WPI Acc No: 1993-370367/199347

Related WPI Acc No: 1992-168370; 1992-383895; 1993-176959; 1993-370175;  
1993-370186; 1993-370368; 1993-370369; 1996-043499; 1996-251401;  
1997-099843; 1997-144354; 1997-201791; 1997-201811; 1997-212476;  
1997-258546; 1997-349671; 1998-100637; 1998-120273; 1998-145157;  
1998-297337; 1998-311882; 1998-332742; 1998-347933; 1998-456661;  
1998-520635; 1998-594399; 1999-153205; 1999-213434; 1999-571471

XRPX Acc No: N93-285952

**Odvanced parallel array processor computer system - has array processor of eight processors on single chip with associated processing element, memory and I-O ,and are interconnected with hypercube based technology**

Patent Assignee: INT BUSINESS MACHINES CORP (IBM )  
Inventor: BARKER T N; COLLINS C A; DAPP M C; DIEFFENDERFER J W; GRICE D G;  
KNOWLES B J; KOGGE P M; KUCHINSKI D C; LESMEISTER D M; MILES R E; NIER R  
E; RETTER E E; RICHARDSON R R; ROLFE D B; SCHOONOVER N J; SMORAL V J;  
STUPP J R; WILKINSON P A

Number of Countries: 004 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 570950	A2	19931124	EP 93108192	A	19930519	199347 B
EP 570950	A3	19940720				199528
US 5590345	A	19961231	US 90611594	A	19901113	199707
			US 91698866	A	19910513	
			US 91798788	A	19911127	
			US 92887630	A	19920522	
US 5710935	A	19980120	US 90611594	A	19901113	199810
			US 91698866	A	19910513	
			US 91798788	A	19911127	
			US 92887630	A	19920522	
			US 95466462	A	19950606	
US 5717943	A	19980210	US 90611594	A	19901113	199813
			US 91698866	A	19910513	
			US 91798788	A	19911127	
			US 92887630	A	19920522	
			US 95465926	A	19950605	
US 5842031	A	19981124	US 90611594	A	19901113	199903
			US 91698866	A	19910513	
			US 91798788	A	19911127	
			US 92887630	A	19920522	
			US 94301278	A	19940906	
			US 95468045	A	19950606	

Priority Applications (No Type Date): US 92887630 A 19920522; US 90611594 A 19901113; US 91698866 A 19910513; US 91798788 A 19911127; US 95466462 A 19950606; US 95465926 A 19950605; US 94301278 A 19940906; US 95468045 A 19950606

Cited Patents: Jnl.Ref; EP 132926; EP 460599; WO 8909967

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 570950	A2	E	84	G06F-015/16	
				Designated States (Regional): DE FR GB	
US 5590345	A		64	G06F-013/00	CIP of application US 90611594 CIP of application US 91698866 CIP of application US 91798788 CIP of patent US 5313645
US 5710935	A		64	G06F-015/80	CIP of application US 90611594 CIP of application US 91698866 CIP of application US 91798788 Div ex application US 92887630 CIP of patent US 5313645 Div ex patent US 5590345
US 5717943	A		71	G06F-015/80	CIP of application US 90611594 CIP of application US 91698866 CIP of application US 91798788 Div ex application US 92887630
US 5842031	A			G06F-015/80	Cont of application US 90611594 CIP of application US 91698866 CIP of application US 91798788 Cont of application US 92887630 CIP of application US 94301278 CIP of patent US 5475856 Cont of patent US 5590345

Abstract (Basic): EP 570950 A

The **computer system** includes **several** processor memory elements on a common substrate. Each of the elements has internal and external communications paths for communication between a number of other processor memory elements on the substrate and for communication with other processing elements external to the substrate.

A node of a processor array has a several single processor elements comprising a network node of eight or more processors with their associated memory with fully distributed I=O routers and signal I=O ports at each of the single processing elements.

USE/ADVANTAGE - for complex scientific and business applications. APAP may be incorporated on single semiconductor silicon chip. Uses only single chip type while reducing chip **boundary** crossings and line **length**.

Dwg.11/27

Title Terms: PARALLEL; ARRAY; PROCESSOR; COMPUTER; SYSTEM; ARRAY; PROCESSOR ; EIGHT; PROCESSOR; SINGLE; CHIP; ASSOCIATE; PROCESS; ELEMENT; MEMORY;

I-O; INTERCONNECT; BASED; TECHNOLOGY

Index Terms/Additional Words: APAP

Derwent Class: T01

International Patent Class (Main): G06F-013/00 ; G06F-015/16 ;

G06F-015/80

File Segment: EPI

11/5/20 (Item 13 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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009635734 \*\*Image available\*\*

WPI Acc No: 1993-329283/199342

XRPX Acc No: N93-254246

**System for loading one of multiple operating systems in computer - has dual boot arrangement for operating system with type preference bit containing boot source location with pen point style loader**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC )

Inventor: KANNAN K; LYBRAND D P; NOVAK F P

Number of Countries: 005 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 565875	A2	19931020	EP 93104155	A	19930315	199342 B
EP 565875	A3	19940518	EP 93104155	A	19930315	199524
US 5454110	A	19950926	US 92869552	A	19920415	199544
			US 94294824	A	19940826	
US 5519870	A	19960521	US 92869552	A	19920415	199626
			US 94294821	A	19940824	
			US 95469627	A	19950606	
JP 2986299	B2	19991206	JP 9325301	A	19930215	200003

Priority Applications (No Type Date): US 92869552 A 19920415; US 94294824 A 19940826; US 94294821 A 19940824; US 95469627 A 19950606

Cited Patents: -SR.Pub; 4.Jnl.Ref; WO 9207319

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
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EP 565875	A2	E	18 G06F-009/44	
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Designated States (Regional): DE FR GB

JP 2986299	B2	14	G06F-001/00	Previous Publ. patent JP 6187133
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US 5454110	A	14	G06F-013/00	Div ex application US 92869552
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US 5519870	A	16	G06F-003/03	Div ex application US 92869552
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Cont of application US 94294821

EP 565875	A3		G06F-009/44	
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Abstract (Basic): EP 565875 A

The system comprises a dual boot arrangement (200) for selecting and loading an operating system (210) from the **multiple operating systems** with an operating identification arrangement to retrieve a selected operating system. The identification arrangement has a non volatile RAM containing an operating system type preference bit (206) containing the type of system to be loaded and a boot source **location** containing a medium from which to retrieve the selected system.

An operating system loader which comprises a DOS type loader is provided which comprises a pen point style loader for a pen point operating system with a DOS compatible file system comprising a **link**

source or a local area network.

USE/ADVANTAGE - Pen based portable computer. Supports frequent and unexpected peripheral use during **operation** of computer.

Dwg.2/6

Title Terms: SYSTEM; LOAD; ONE; MULTIPLE; OPERATE; SYSTEM; COMPUTER; DUAL; BOOT; ARRANGE; OPERATE; SYSTEM; TYPE; PREFER; BIT; CONTAIN; BOOT; SOURCE; LOCATE; PEN; POINT; STYLE; LOAD

Index Terms/Additional Words: BIOS; ABIOS; DOS; firmware

Derwent Class: T01

International Patent Class (Main): G06F-001/00 ; G06F-003/03 ; G06F-009/44 ; G06F-013/00

International Patent Class (Additional): G06F-003/033 ; G06F-009/06

File Segment: EPI

11/5/21 (Item 14 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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009483424 \*\*Image available\*\*

WPI Acc No: 1993-176959/199322

Related WPI Acc No: 1992-168370; 1992-383895; 1993-370175; 1993-370186; 1993-370367; 1993-370368; 1993-370369; 1996-043499; 1996-251401; 1997-099843; 1997-144354; 1997-201791; 1997-201811; 1997-212476; 1997-258546; 1997-349671; 1998-100637; 1998-120273; 1998-145157; 1998-297337; 1998-311882; 1998-332742; 1998-347933; 1998-456661; 1998-520635; 1998-594399; 1999-153205; 1999-213434; 1999-571471; 1999-580053

XRPX Acc No: N93-135620

**Dynamic multi-mode parallel processor array architecture computer system**  
**- includes multiple groups of processors and memories and interconnection path between processors**

Patent Assignee: IBM CORP (IBMC ); INT BUSINESS MACHINES CORP (IBMC )

Inventor: KOGGE P M

Number of Countries: 016 Number of Patents: 008

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 544127	A2	19930602	EP 92118887	A	19921104	199322 B
CA 2073516	A	19930528	CA 2073516	A	19920709	199333
CN 1072788	A	19930602	CN 92111552	A	19921020	199412
EP 544127	A3	19940420				199523
US 5475856	A	19951212	US 91798788	A	19911127	199604
			US 94324295	A	19941017	
EP 544127	B1	19990310	EP 92118887	A	19921104	199914
DE 69228586	E	19990415	DE 628586	A	19921104	199921
			EP 92118887	A	19921104	
KR 9708529	B1	19970524	KR 9220971	A	19921109	199943

Priority Applications (No Type Date): US 91798788 A 19911127; US 94324295 A 19941017

Cited Patents: -SR.Pub; 1.Jnl.Ref; US 4873626

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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EP 544127	A2	E	19	G06F-015/16	
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Designated States (Regional): AT BE CH DE ES FR GB IE IT LI NL SE

US 5475856	A	16	G06F-013/00	Cont of application	US 91798788
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EP 544127	B1	E	G06F-015/16		
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Designated States (Regional): AT BE CH DE ES FR GB IE IT LI NL SE

DE 69228586	E	G06F-015/16	Based on patent	EP 544127
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CA 2073516	A	G06F-015/80		
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CN 1072788	A	G06F-009/00		
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KR 9708529	B1	G06F-015/16		
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Abstract. (Basic): EP 544127 A

The **computer system** comprises **multiple** groups of processors and memories and an interconnection path between processors. An operating system controls the **execution** of **instructions** by the



processors of the system.

The operating system enables groups of processors to be dynamically configured to operate as either MIMD, SIMD or SISD groups of processors, with dynamic configuration by change of modes for executing **instructions** of one or more programs. The change of modes is enabled on an **instruction** by **instruction** basis and at least some of the processors are physically identical and yet perform multi-mode **functions**.

USE/ADVANTAGE - Broadcast/switching appts. multi-sender switching etc. Enables point to point coupling of processors without **blocking**.

Dwg.1/5

Title Terms: DYNAMIC; MULTI; MODE; PARALLEL; PROCESSOR; ARRAY; ARCHITECTURE  
; COMPUTER; SYSTEM; MULTIPLE; GROUP; PROCESSOR; MEMORY; INTERCONNECT;  
PATH; PROCESSOR

Index Terms/Additional Words: RISC; SIMD; MIMD; SISD

Derwent Class: T01

International Patent Class (Main): G06F-009/00 ; G06F-013/00 ;

G06F-015/16 ; G06F-015/80

International Patent Class (Additional): G06F-007/00

File Segment: EPI

11/5/22 (Item 15 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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008835996 \*\*Image available\*\*

WPI Acc No: 1991-340013/199146

XRPX Acc No: N91-260463

**Integrated circuit I-O using high performance bus interface - has fewer bus lines than number of bits in single address without individual device select lines**

Patent Assignee: RAMBUS INC (RAMB-N); FARMWALD M (FARM-I); HOROWITZ M (HORO-I); RAMBUS (RAMB-N)

Inventor: FARMWALD M; HOROWITZ M; HOROWITZ M A

Number of Countries: 019 Number of Patents: 087

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9116680	A	19911031				199146	B
EP 525068	A1	19930203	EP 91908374	A	19910416	199305	
			WO 91US2590	A	19910416		
US 5243703	A	19930907	US 90510898	A	19900418	199337	
			US 92849211	A	19920305		
JP 5507374	W	19931021	JP 91508050	A	19910416	199347	
			WO 91US2590	A	19910416		
US 5319755	A	19940607	US 90510898	A	19900418	199422	
			US 92954945	A	19920930		
US 5408129	A	19950418	US 90510898	A	19900418	199521	
			US 92847112	A	19920305		
			US 94183573	A	19940118		
IL 110649	A	19950831	IL 110649	A	19901227	199543	
US 5473575	A	19951205	US 90510898	A	19900418	199603	
			US 92847532	A	19920305		
IL 110648	A	19951208	IL 110648	A	19901227	199612	
US 5499385	A	19960312	US 90510898	A	19900418	199616	
			US 92849212	A	19920305		
EP 525068	A4	19950920	EP 91908374	A		199619	
IL 110650	A	19960331	IL 110650	A	19901227	199622	
IL 96808	A	19960331	IL 96808	A	19901227	199622	
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			Div ex patent US 5841580
			patent
US 20020147877 A1	G06F-013/14		Cont of application US 90510898
			Cont of application US 92954945
			Div ex application US 94222646
			Div ex application US 95448657
			Div ex application US 97798520
			Cont of application US 98161090
			Cont of application US 2000545648
			Cont of application US 2001835263
			Cont of patent US 5319755
			Div ex patent US 5513327
			Div ex patent US 5638334
			Div ex patent US 5841580
			patent
US 20020147877 A1	G06F-013/14		Cont of application US 90510898
			Cont of application US 92954945
			Div ex application US 94222646
			Div ex application US 95448657
			Div ex application US 97798520
			Cont of application US 98161090
			Cont of application US 2000545648
			Cont of application US 2001835263
			Cont of patent US 5319755
			Div ex patent US 5513327
			Div ex patent US 5638334
			Div ex patent US 5841580
			patent
US 20020147877 A1	G06F-013/14		Cont of application US 90510898
			Cont of application US 92954945
			Div ex application US 94222646
			Div ex application US 95448657
			Div ex application US 97798520
			Cont of application US 98161090
			Cont of application US 2000545648
			Cont of application US 2001835263
			Cont of patent US 5319755
			Div ex patent US 5513327
			Div ex patent US 5638334
			Div ex patent US 5841580
			patent
US 20020147877 A1	G06F-013/14		Cont of application US 90510898
			Cont of application US 92954945
			Div ex application US 94222646
			Div ex application US 95448657
			Div ex application US 97798520
			Cont of application US 98161090
			Cont of application US 2000545648
			Cont of application US 2001835263
			Cont of patent US 5319755
			Div ex patent US 5513327
			Div ex patent US 5638334
			Div ex patent US 5841580
			patent
US 6598171 B1	G11C-008/04		Div ex application US 90510898
			Cont of application US 92847692
			Div ex application US 96749729
			Div ex patent US 5657481

Semiconductor devices (15,16,17) are connected in parallel to a bus (18) which carries **address**, data and control information to the memory devices (15,16,17). Control information includes device-select information and the bus (18) has fewer bus lines than the number of bits in a single **address**. The bus carries device-select information without the need for separate device select lines to the individual devices.

Master and slave devices communicate using a **defined** protocol over the bus (18). Internal registers differentiate each device and allow bus requests to be directed to single or all devices (15,16,17).

USE/ADVANTAGE - In bus interfaces for computer and video systems. Allows high speed transfer of **blocks** of data with low power consumption and high reliability. (124pp Dwg.No.3/15)

Title Terms: INTEGRATE; CIRCUIT; I-O; HIGH; PERFORMANCE; BUS; INTERFACE; BUS; LINE; NUMBER; BIT; SINGLE; **ADDRESS**; INDIVIDUAL; DEVICE; SELECT; LINE

Derwent Class: T01

International Patent Class (Main): G06F-001/04 ; G06F-001/12 ; G06F-012/00 ; G06F-012/02 ; G06F-013/00 ; G06F-013/14 ; G06F-013/16 ; G06F-013/28 ; G06F-013/38 ; G06F-013/40 ; G11C-003/00; G11C-007/00; G11C-008/00; G11C-008/04; G11C-011/401; G11C-011/407; H01L-029/48; H03K-019/003

International Patent Class (Additional): G06F-001/10 ; G06F-012/06 ; G06F-012/56 ; G06F-013/36 ; G06F-013/376 ; G11C-007/06; G11C-007/22; G11C-011/406; H01L-029/44; H01L-029/52; H01L-029/60

File Segment: EPI

11/5/23 (Item 16 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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008750527 \*\*Image available\*\*

WPI Acc No: 1991-254543/199135

XRPX Acc No: N91-194141

**Neural network shell for application programs - provides standard interface to neural networks and organises selection, training and operation**

Patent Assignee: IBM CORP (IBMC ); INT BUSINESS MACHINES CORP (IBMC )

Inventor: BIGUS J P

Number of Countries: 010 Number of Patents: 012

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 443976	A	19910828	EP 91480011	A	19910225	199135 B
US 5142665	A	19920825	US 90482450	A	19900220	199237
US 5222196	A	19930622	US 90482450	A	19900220	199326
			US 92849116	A	19920310	
EP 443976	A3	19930526	EP 91480011	A	19910125	199403
US 5450529	A	19950912	US 90482450	A	19900220	199542
			US 92849116	A	19920310	
			US 9375370	A	19930611	
US 5611020	A	19970311	US 90482450	A	19900220	199716
			US 92849116	A	19920310	
			US 9375370	A	19930611	
			US 95459061	A	19950602	
US 5613040	A	19970318	US 90482450	A	19900220	199717
			US 92849116	A	19920310	
			US 9375370	A	19930611	
			US 95460351	A	19950602	
US 5613043	A	19970318	US 90482450	A	19900220	199717
			US 92849116	A	19920310	
			US 9375370	A	19930611	
			US 95459213	A	19950602	
US 5615306	A	19970325	US 90482450	A	19900220	199718
			US 92849116	A	19920310	
			US 9375370	A	19930611	
			US 95459053	A	19950602	

US 5615307	A	19970405	US 90482450	A	19900220	199718
			US 92849116	A	19920310	
			US 9375370	A	19930611	
			US 95460361	A	19950602	
US 5617511	A	19970401	US 90482450	A	19900220	199719
			US 92849116	A	19920310	
			US 9375370	A	19930611	
			US 95459858	A	19950602	
US 5619618	A	19970408	US 90482450	A	19900220	199720
			US 92849116	A	19920310	
			US 9375370	A	19930611	
			US 95459983	A	19950602	

Priority Applications (No Type Date): US 90482450 A 19900220; US 92849116 A 19920310; US 9375370 A 19930611; US 95459061 A 19950602; US 95460351 A 19950602; US 95459213 A 19950602; US 95459053 A 19950602; US 95460361 A 19950602; US 95459858 A 19950602; US 95459983 A 19950602

Cited Patents: NoSR.Pub; 4.Jnl.Ref

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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EP 443976	A				
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Designated States (Regional): CH DE ES FR GB IT LI NL SE

US 5142665	A	34	G06F-015/18	
US 5222196	A	34	G06F-015/18	Div ex application US 90482450
				Div ex patent US 5142665
US 5450529	A	35	G06F-015/18	Div ex application US 90482450
				Div ex application US 92849116
				Div ex patent US 5142665
				Div ex patent US 5222196
US 5611020	A	35	G06F-015/18	Div ex application US 90482450
				Div ex application US 92849116
				Div ex application US 9375370
				Div ex patent US 5142665
				Div ex patent US 5222196
				Div ex patent US 5450529
US 5613040	A	35	G06F-015/18	Div ex application US 90482450
				Div ex application US 92849116
				Div ex application US 9375370
				Div ex patent US 5142665
				Div ex patent US 5222196
				Div ex patent US 5450529
US 5613043	A	34	G06F-015/18	Div ex application US 90482450
				Div ex application US 92849116
				Div ex application US 9375370
				Div ex patent US 5142665
				Div ex patent US 5222196
				Div ex patent US 5450529
US 5615306	A	35	G06F-015/18	Div ex application US 90482450
				Div ex application US 92849116
				Div ex application US 9375370
				Div ex patent US 5142665
				Div ex patent US 5222196
				Div ex patent US 5450529
US 5615307	A	35	G06F-015/18	Div ex application US 90482450
				Div ex application US 92849116
				Div ex application US 9375370
				Div ex patent US 5142665
				Div ex patent US 5222196
				Div ex patent US 5450529
US 5617511	A	34	G06F-015/18	Div ex application US 90482450
				Div ex application US 92849116
				Div ex application US 9375370
				Div ex patent US 5142665
				Div ex patent US 5222196
				Div ex patent US 5450529
US 5619618	A	35	G06F-015/18	Div ex application US 90482450
				Div ex application US 92849116

Div ex application 9375370  
Div ex patent US 5142665  
Div ex patent US 5222196  
Div ex patent US 5450529

Abstract (Basic): EP 443976 A

A neutral network shell (32) provides a **defined** interface (31) to application programs. Through this interface any application program becomes a neutral network application program. The shell contains utilises (33) to transfer data to and from the neutral network (50). These utilises **define** new neutral network models, create data structures, train the network and allow it to be run.

Once trained the neutral network can be transported to other computer systems using different languages and different operating systems.

USE/ADVANTAGE - Allows non-experts in neutral networks to use and manage neutral network models.

Dwg.3a/20

Title Terms: NEURAL; NETWORK; SHELL; APPLY; PROGRAM; STANDARD; INTERFACE;  
NEURAL; NETWORK; ORGANISE; SELECT; TRAINING; OPERATE

Derwent Class: T01

International Patent Class (Main): G06F-015/18

International Patent Class (Additional): G06F-015/80

File Segment: EPI

11/5/24 (Item 17 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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008735503 \*\*Image available\*\*

WPI Acc No: 1991-239519/199133

XRPX Acc No: N91-182656

**Multiprocessor system sharing common memory - uses memory controller connected to main memory having memory management table that defines address for copying operation**

Patent Assignee: HITACHI LTD (HITA )

Inventor: FUKAGAWA M; ISOBE T

Number of Countries: 002 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 4103093	A	19910808	DE 4103093	A	19910201	199133 B
US 5293602	A	19940308	US 91647513	A	19910128	199410
DE 4103093	C2	19980528	DE 4103093	A	19910201	199825

Priority Applications (No Type Date): JP 9023310 A 19900201

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 4103093	A		12		
US 5293602	A		12	G06F-013/14	
DE 4103093	C2			G06F-015/16	

Abstract (Basic): DE 4103093 A

The multiprocessor system (SP0,SP1) connects to a memory controller (SC) connected to a shared main memory. Each processor module has a buffer memory (PS0,PS1) to store copies of the data in the main memory (4) and a buffer **address** field (11a,11b).

The memory controller has a second memory management table (FAF0,FAF1) that **defines** the **address** for the copying **operation**. The unit also has a third table (DAF) containing part of the data relating to the operand data of the copy.

ADVANTAGE - Enables efficient transfer of data between processors and common memory.

Dwg.1/5

Title Terms: MULTIPROCESSOR; SYSTEM; SHARE; COMMON; MEMORY; MEMORY; CONTROL  
; CONNECT; MAIN; MEMORY; MEMORY; MANAGEMENT; TABLE; **DEFINE** ; **ADDRESS** ;  
COPY; OPERATE

Derwent Class: T01

International Patent Class (Main): G06F-013/14 ; G06F-015/16

International Patent Class (Additional): G06F-009/46 ; G06F-012/08

File Segment: EPI

11/5/25 (Item 18 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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008293399 \*\*Image available\*\*

WPI Acc No: 1990-180400/199024

XRPX Acc No: N90-140215

**Memory management in fault tolerant multi-processor systems - has private memory areas as part of shared, and voted, main memories**

Patent Assignee: TANDEM COMPUTERS INC (TAND ); TANDEM COMPUTERS IN (TAND-N)

Inventor: ALLISON J; CUTTS R; DEBACKER K; HORST R; JEWETT D; MEHTA N; PEET C; CUTTS R W; JEWETT D E; MEHTA N A; ALLISON J D; DEBACKER K C; HORST R W ; PEET C E

Number of Countries: 015 Number of Patents: 010

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 372578	A	19900613	EP 89122707	A	19891208	199024 B
CA 2003342	A	19900609				199034
US 4965717	A	19901023	US 88283573	A	19881213	199045
EP 447578	A	19910925	EP 90105103	A	19900319	199139 N
AU 9052027	A	19910926				199146 N
US 5146589	A	19920908	US 88282540	A	19881209	199239
			US 90629698	A	19901217	
EP 372578	A3	19920115	EP 89122707	A	19891208	199321
US 4965717	B	19930525	US 88283573	A	19881213	199322
US 5388242	A	19950207	US 88282469	A	19881209	199512
			US 92982074	A	19921124	
US 5758113	A	19980526	US 88282540	A	19881209	199828
			US 90629698	A	19901217	
			US 92928555	A	19920811	
			US 97815997	A	19970310	

Priority Applications (No Type Date): US 88283573 A 19881213; US 88282469 A 19881209; US 88282540 A 19881209; EP 90105103 A 19900319; US 90629698 A 19901217; US 92982074 A 19921124; US 92928555 A 19920811; US 97815997 A 19970310

Cited Patents: NoSR.Pub; 4.Jnl.Ref; DE 3216238; EP 104490; EP 286856; JP 57089163; JP 61265660; JP 62135940; US 3921149; WO 8502698

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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EP 372578	A		39		
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Designated States (Regional): AT DE FR GB IT SE

US 4965717	A		31		
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EP 447578	A				
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Designated States (Regional): BE CH ES LI LU NL

US 5146589	A		31	G06F-012/00	Cont of application US 88282540
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EP 372578	A3		39		
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US 4965717	B		2	G06F-011/18	
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US 5388242	A		30	G06F-012/02	Cont of application US 88282469
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US 5758113	A			G06F-012/00	Cont of application US 88282540
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Cont of application US 90629698

Cont of application US 92928555

Cont of patent US 5146589

Abstract (Basic): EP 372578 A

The fault-tolerant computer system has identical CPU's (11,12,13) executing the same **instruction stream**, and multiple self-checking memory modules (14,15). I/O **functions** are implemented by two identical buses and a pair of I/O processors connected to I/O devices. The CPU's have their own local 8MByte memory and can also assign part

of the common 32MByte memory for private use. The area of shared memory used privately by a processor can be dynamically reassigned, but can only be written to by 'private memory write' commands. Each processor accesses its own private memory in the shared area.

When a 'private write' command occurs, the address and write command are still voted, as for all writes, but the memory address is altered to select the relevant private area.

USE/ADVANTAGE - Provides multiple processors with means of communication non-identical data to each other. (39pp Dwg.No.1/22

Title Terms: MEMORY; MANAGEMENT; FAULT; TOLERATE; MULTI; PROCESSOR; SYSTEM; PRIVATE; MEMORY; AREA; PART; SHARE; MAIN; MEMORY

Derwent Class: T01

International Patent Class (Main): G06F-011/18 ; G06F-012/00 ;

G06F-012/02

International Patent Class (Additional): G06F-011/16 ; G06F-012/08 ;

G06F-013/00 ; G06F-015/16 ; G06F-015/76

File Segment: EPI

11/5/26 (Item 19 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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008291937 \*\*Image available\*\*

WPI Acc No: 1990-178938/199023

XRPX Acc No: N90-139067

Virtual computer system having extended memory - has first converter for reading virtual physical ES address and second for generating physical ES address

Patent Assignee: HITACHI LTD (HITA )

Inventor: HARAGUCHI M; OGAWA K; SAIJO K; TAKEDA K; TANAKA S; UMEMO H;

YAMAOKA A; ASUMURA K

Number of Countries: 002 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9005338	A	19900517				199023 B
DE 3991303	T	19901122	DE 3991003	A	19890928	199048 N
US 5341484	A	19940823	WO 89JP983	A	19890928	199433
			US 90476434	A	19900524	

Priority Applications (No Type Date): JP 89131348 A 19890526; JP 88276252 A 19881102; DE 3991003 A 19890928

Cited Patents: JP 61098461; JP 63244152

Patent Details:

Patent No	Kind	Int	Pg	Main IPC	Filing Notes
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WO 9005338	A				
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Designated States (National): DE US

US 5341484	A	26	G06F-012/00	Based on patent WO 9005338
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Abstract (Basic): WO 9005338 A

A virtual computer system has an extended memory which permits the running of a number of operating systems (OS) on one computer having main memory and at least one extended memory and which includes at least one virtual main memory which permits each of the plurality of OSs to reside on main memory. At least one virtual extended memory (virtual ES) resides on the extended memory.

A first convertor reads a virtual physical ES address on the virtual extended memory corresponding to the virtual ES address from a virtual ES address on the virtual space of the virtual ES designated by one of the number of OSs and from an address inside a relocation table for the extended memory on the virtual main memory of one OS or inside a register of a computer. A second convertor generates a physical ES address on the physical extended memory corresponding to the virtual physical address from a virtual physical ES address and from the start address at the physical ES on at least one extended memory on which the virtual ES of one OS always reside. (66pp Dwg.No.23/21)

Title Terms: VIRTUAL; COMPUTER; SYSTEM; EXTEND; MEMORY; LIST; CONVERTER;  
READ; VIRTUAL; PHYSICAL; ADDRESS ; SECOND; GENERATE; PHYSICAL; ADDRESS  
Derwent Class: T01  
International Patent Class (Additional): G06F-009/46 ; G06F-012/10  
File Segment: EPI

11/5/27 (Item 20 from file: 350)  
DIALOG(R) File 350:Derwent WPIX  
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008000060 \*\*Image available\*\*  
WPI Acc No: 1989-265172/198937  
XRPX Acc No: N89-202227

Capability domain control appts. for computer system - has access  
registers each contg. access list entry token to signify address space  
for which general purpose register is to be allowed access

Patent Assignee: IBM CORP (IBM ) ; INT BUSINESS MACHINES CORP (IBM )  
Inventor: CLARK C E; GANEK A G; MALL M G; PAGE D R  
Number of Countries: 006 Number of Patents: 006  
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 331900	A	19890913	EP 89101790	A	19890202	198937 B
BR 8900567	A	19891010				198946
US 4945480	A	19900731	US 88154685	A	19880210	199033
CA 1293811	C	19911231				199208
EP 331900	B1	19951108	EP 89101790	A	19890202	199549
DE 68924720	E	19951214	DE 624720	A	19890202	199604
			EP 89101790	A	19890202	

Priority Applications (No Type Date): US 88154685 A 19880210  
Cited Patents: No-SR.Pub; 2.Jnl.Ref; EP 176939; EP 76097; US 4145738; US  
4355355; US 4500952

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 331900	A	E	41		
Designated States (Regional): DE FR GB					
EP 331900	B1	E	44	G06F-009/46	
Designated States (Regional): DE FR GB					
DE 68924720	E			G06F-009/46	Based on patent EP 331900

Abstract (Basic): EP 331900 A

The apparatus translates the contents of access registers into information for use in performing **addressing functions** for multiple virtual **address** spaces. The access registers represent the full register **addressing** capability of the system but do not directly contain the **addressing** information. The system has a number of general purpose registers and access registers associated with the general registers. An access list has access list entries which is **addressed** by the contents of the access register. A memory storage holds **address** space number second table entries (ASTE), where the contents of the access list entry locate the ASTE and where the ASTE contains the **addressing** information needed to locate a virtual **address** when combined with the contents of a general register. Access res translation (ART) consists of the process of determining **addressing** information by using the access list entry and the ASTE.

The system has available to it at any one time a selection of one of two domains each represented by an access list. One **domain** is related to the dispatchable unit tasks to be performed and the other is related to the **address** space in which a particular program operates. The ART process selects the **domain** which the access register is using.

Title Terms: CAPABLE; DOMAIN ; CONTROL; APPARATUS; COMPUTER; SYSTEM;  
ACCESS; REGISTER; CONTAIN; ACCESS; LIST; ENTER; TOKEN; SIGNIFY; ADDRESS  
; SPACE; GENERAL; PURPOSE; REGISTER; ALLOW; ACCESS  
Derwent Class: T01  
International Patent Class (Main): G06F-009/46



International Patent Class (Additional): G06F-012/06 ; G06F-012/08 ;  
G06F-012/10  
File Segment: EPI

11/5/28 (Item 21 from file: 350)  
DIALOG(R) File 350:Derwent WPIX  
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007970095  
WPI Acc No: 1989-235207/198933  
XRPX Acc No: N89-179195

**Mechanism for zero-origin data spaces in data processing system - allows entire virtual addressing range to be available to programs to use for data isolation and data sharing**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC ); IBM CORP (IBMC )  
Inventor: SCALZI C A; SCHMALZ R J; SCHMAIZ R J  
Number of Countries: 005 Number of Patents: 005  
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 327798	A	19890816	EP 89100131	A	19890105	198933 B
BR 8900603	A	19891010				198946
US 5008811	A	19910416	US 88134688	A	19880210	199118
EP 327798	B1	19950802	EP 89100131	A	19890105	199535
DE 68923627	E	19950907	DE 623627	A	19890105	199541
			EP 89100131	A	19890105	

Priority Applications (No Type Date): US 88154688 A 19880210; US 88134688 A 19880210

Cited Patents: 1.Jnl.Ref; A3...9048; No-SR.Pub; US 4096573; US 4145738; US 4042911

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 327798	A	E	10		
Designated States (Regional): DE FR GB					
EP 327798	B1	E	27	G06F-012/10	
Designated States (Regional): DE FR GB					
DE 68923627	E			G06F-012/10	Based on patent EP 327798

Abstract (Basic): EP 327798 A

A control method and mechanism for zero-origin data spaces. The mechanism for supporting two distinct **address** space types in a central processing complex comprising a CPU, main storage, system resources connected to the CPU and to the main storage and an **operating system** supporting **several address spaces** containing **instructions** and data involves the following. A program **address** space type in which at least one segment of storage is common to all such **address** space types and at least one segment of storage is unique to a particular **address** space type and a data space type in which all segments of storage are unique to each **address** space of such an **address** space type.

A system for resolving virtual **addresses** within one of the **address** spaces into real **addresses** within main system storage by a dynamic look aside table having entries comprising virtual **addresses** and corresponding real **addresses**, the entries are useable for bypassing the system for resolving virtual **addresses** and for distinguishing between program **address** spaces which permit sharing of entries among **address** spaces of the **described address** type. For **addresses** within common segments and data spaces, which do not permit sharing of entries.

USE/ADVANTAGE - For supporting data space without common segments in addition to traditional **address** spaces containing common segments with data processing system. Permits entire virtual **addressing** range to be available to programs wishing to use such data spaces for data isolation and data sharing.

Title Terms: MECHANISM; ZERO; ORIGIN; DATA; SPACE; DATA; PROCESS; SYSTEM; ALLOW; VIRTUAL; **ADDRESS** ; RANGE; AVAILABLE; PROGRAM; DATA; ISOLATE; DATA

.; SHARE

Derwent Class: T01

International Patent Class (Main): G06F-012/10

International Patent Class (Additional): G06F-009/00 ; G06F-012/14

File Segment: EPI

11/5/29 (Item 22 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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007894558 \*\*Image available\*\*

WPI Acc No: 1989-159670/198922

XRPX Acc No: N89-121731

Address conversion procedure in virtual memory computer - uses  
addressing registers as basis for generation of physical addresses to  
allow normal access and privileged access

Patent Assignee: NEC CORP (NIDE )

Inventor: YOKOYAMA Y

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
FR 2621719	A	19890414	FR 8813270	A	19881010	198922 B
US 5107417	A	19920421	US 88255603	A	19881011	199219

Priority Applications (No Type Date): JP 87252362 A 19871008

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
FR 2621719	A		14		
US 5107417	A		7		

Abstract (Basic): FR 2621719 A

The address conversion procedure comprises a sequence of  
operations for conversion of a virtual address in a computer to a  
physical address. The sequence of operations is as follows: an  
effective address is generated using address registers; a decision  
concerning the operating mode is taken to determine whether or not a  
process is active; a decision, based on the outcome of the preceding  
step, is taken to decide whether or not a register comprising a  
specific reference number was used during address generation.

A memory access is made, based on an affirmative outcome from  
previous stage, which uses an effective address from the first stage.  
The effective address is appropriate to any physical address.

USE/ADVANTAGE - Reduced loss of time in memory access in virtual  
memory computer system which allows multiple processes, giving in  
particular easy control of privileged processes.

2/3

Title Terms: ADDRESS ; CONVERT; PROCEDURE; VIRTUAL; MEMORY; COMPUTER;  
ADDRESS ; REGISTER; BASIS; GENERATE; PHYSICAL; ADDRESS ; ALLOW; NORMAL;  
ACCESS; ACCESS

Derwent Class: T01

International Patent Class (Additional): G06F-009/30 ; G06F-012/08 ;

G06F-013/00

File Segment: EPI

11/5/30 (Item 23 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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007688948 \*\*Image available\*\*

WPI Acc No: 1988-322880/198845

XRPX Acc No: N88-244932

Exclusive read-modify-write operations executer for pended bus - uses  
responder node in multiprocessor having multiple lock bits, and lock  
status control circuit

Patent Assignee: NIPPON DIGITAL EQUIP KK (DIGI )

Inventor: GILLET R B; WILLIAMS D D  
Number of Countries: 016 Number of Patents: 008  
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 8808584	A	19881103	WO 88US1299	A	19880425	198845 B
AU 8817168	A	19881202				198908
EP 344216	A	19891206	EP 88904314	A	19880425	198949
JP 2500783	W	19900315				199017
US 4949239	A	19900814	US 8744466	A	19870501	199035
CA 1304828	C	19920707	CA 565480	A	19880429	199233
EP 344216	B1	19930804	EP 88904314	A	19880425	199331
			WO 88US1299	A	19880425	
DE 3882977	G	19930909	DE 3882977	A	19880425	199337
			EP 88904314	A	19880425	
			WO 88US1299	A	19880425	

Priority Applications (No Type Date): US 8744466 A 19870501

Cited Patents: EP 138676; GB 2044499; US 4115854

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
WO 8808584	A	E 44		
				Designated States (National): AU JP KR
				Designated States (Regional): AT BE CH DE FR GB IT LU NL SE
EP 344216	A	E		
				Designated States (Regional): CH DE FR GB IT LI NL SE
EP 344216	B1	E 29	G06F-013/42	Based on patent WO 8808584
				Designated States (Regional): CH DE FR GB IT LI NL SE
DE 3882977	G		G06F-013/42	Based on patent EP 344216
				Based on patent WO 8808584
CA 1304828	C		G06F-013/42	

Abstract (Basic): WO 8808584 A

The memory (39) is arranged to act as a responder node. A bus interface (64) acts with input queue (306), **command** decode and **address** and parity check circuit (300), **address** register (302), acknowledge indication generator (304) and internal lines, for sending acknowledge indications to processor nodes after a given number of bus cycles subsequent to a **command** message.

A **command** decoder (308) removes stored messages from the input queue and generates interlock read and unlock write **commands** and **address** data from the messages. A lock controller (310) permits access to the memory array (312) in an unlocked condition and prevents access to the array in a locked condition.

ADVANTAGE - Lock status information is not transferred with fixed time relationship to initial interlock read **command**.

8/9

Title Terms: EXCLUDE; READ; MODIFIED; WRITING; OPERATE; BUS; RESPOND; NODE; MULTIPROCESSOR; MULTIPLE; LOCK; BIT; LOCK; STATUS; CONTROL; CIRCUIT

Derwent Class: T01

International Patent Class (Main): G06F-013/42

International Patent Class (Additional): G06F-009/46 ; G06F-013/18 ;

G06F-015/16

File Segment: EPI

11/5/31 (Item 24 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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007688936 \*\*Image available\*\*

WPI Acc No: 1988-322868/198845

XRPX Acc No: N88-244920

Initiating transactions on multi-process computer system - sending interlock read command to appropriate node in memory when processor wishes to modify memory contents

Patent Assignee: DIGITAL EQUIP CORP (DIGI )

Inventor: GILLET R B; WILLIAMS D D

Number of Countries: 01 Number of Patents: 009

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 8808571	A	19881103	WO 88US1359	A	19880422	198845 B
AU 8817250	A	19881202				198908
JP 1502628	W	19890907	JP 88504143	A	19880422	198942
EP 358690	A	19900321	EP 88904323	A	19880422	199012
US 4941083	A	19900710	US 8744486	A	19870501	199030
CA 1303233	C	19920609	CA 565200	A	19880427	199229
EP 358690	B1	19930804	EP 88904323	A	19880422	199331
			WO 88US1359	A	19880422	
DE 3882988	G	19930909	DE 3882988	A	19880422	199337
			EP 88904323	A	19880422	
			WO 88US1359	A	19880422	
KR 9300992	B1	19930212	WO 88US1359	A	19880422	199417
			KR 88701790	A	19881229	

Priority Applications (No Type Date): US 8744486 A 19870501

Cited Patents: EP 138676; GB 2044499

Patent Details:

Patent No	Kind	lan	Pg	Main IPC	Filing Notes
WO 8808571	A	E	39		
				Designated States (National):	AU JP KR
				Designated States (Regional):	AT BE CH DE FR GB IT LU NL SE
EP 358690	A	E			
				Designated States (Regional):	CH DE FR GB IT LI NL SE
EP 358690	B1	E	27	G06F-009/46	Based on patent WO 8808571
				Designated States (Regional):	CH DE FR GB IT LI NL SE
DE 3882988	G			G06F-009/46	Based on patent EP 358690
					Based on patent WO 8808571
CA 1303233	C			G06F-009/46	
KR 9300992	B1			G06F-009/46	

Abstract (Basic): WO 8808571 A

Memory in a multiprocessor computer system is accessed using a method which regulates the access and reduces contention. When a processor wishes to modify the contents of a memory **location** it sends an interlock read **command** to the appropriate node in the memory. Receipt of this is promptly acknowledged and it is placed in a queue to be processed.

When its turn comes, if there is a **block** in that **location** it sends a message to that effect, if not it sends the required data and puts a lock on which will prevent access by another processor. When the modified data is sent back the lock is removed. Thus the exact **location** needed is **blocked** and contention reduced to a minimum.

ADVANTAGE - By setting lock on **specific location** and only against modifying access, problems from contention are reduced to minimum.

Dwg.8/9

Title Terms: INITIATE; TRANSACTION; MULTI; PROCESS; COMPUTER; SYSTEM; SEND; INTERLOCKING; READ; **COMMAND** ; APPROPRIATE; NODE; MEMORY; PROCESSOR; MODIFIED; MEMORY; CONTENT

Derwent Class: T01

International Patent Class (Main): **G06F-009/46**

International Patent Class (Additional): **G06F-013/42 ; G06F-015/16**

File Segment: EPI

11/5/32 (Item 25 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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007688934 \*\*Image available\*\*

WPI Acc No: 1988-322866/198845

XRPX Acc No: N88-244918

**Multi-lock indicator managing appts. for multi-processor computer - has memory for accessing pended bus, and transmits response message including**

6 0 , contents of specified location stored in output queue

Patent Assignee: DIGITAL EQUIP CORP (DIGI )

Inventor: GILLET R B; WILLIAMS D D

Number of Countries: 017 Number of Patents: 010

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 8808569	A	19881103	WO 88US1297	A	19880427	198845 B
AU 8817285	A	19881202				198908
US 4858116	A	19890815	US 8744954	A	19870501	198941
EP 358703	A	19900321	EP 88904805	A	19880427	199012
JP 2500550	W	19900222	JP 88504366	A	19880427	199014
US 5068781	A	19911126	US 89372565	A	19890628	199150
CA 1304167	C	19920623	CA 565473	A	19880429	199231
EP 358703	B1	19930804	EP 88904801	A	19880427	199331
			WO 88US1297	A	19880427	
DE 3882989	G	19930909	DE 3882989	A	19880427	199337
			EP 88904801	A	19880427	
			WO 88US1297	A	19880427	
KR 9210915	B1	19921224	WO 88US1297	A	19880427	199415
			KR 88701742	A	19881228	

Priority Applications (No Type Date): US 8744954 A 19870501

Cited Patents: EP 121700; EP 138676; US 4115854; GB 2044499

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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WO 8808569	A	E	50		
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Designated States (National): AU JP KR

Designated States (Regional): AT BE CH DE FR GB IT LU NL SE

US 4858116	A		22		
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EP 358703	A	E			
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Designated States (Regional): CH DE FR GB IT LI NL SE

EP 358703	B1	E	31	G06F-009/46	Based on patent WO 8808569
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Designated States (Regional): CH DE FR GB IT LI NL SE

DE 3882989	G			G06F-009/46	Based on patent EP 358703
					Based on patent WO 8808569

CA 1304167	C			G06F-009/46	
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KR 9210915	B1			G06F-009/46	
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Abstract (Basic): WO 8808569 A

The **computer system** has **several** processors interconnected by a pended bus (25) and provides exclusive read-modify-write **operations** using multiple lock bits. A processor generates an interlock read **command** which is transmitted as a transfer over the pended bus to a memory or I/O node. Acknowledge confirmations are transmitted by the memory back to the 2 processor two cycles after each bus cycle of the processor transfer.

The processor transfer, including an interlock read **command**, is stored in an input queue (306) in memory and processes in turn by the memory. An interlock read **command** to a **specified** memory **location** causes a lock bit to be set for the **location** and a first type of response message including the contents of the **specified** **location** to be generated by the memory and stored in an input queue (318).

Dwg.8/9

Title Terms: MULTI; LOCK; INDICATE; MANAGE; APPARATUS; MULTI; PROCESSOR; COMPUTER; MEMORY; ACCESS; BUS; TRANSMIT; RESPOND; MESSAGE; CONTENT; **SPECIFIED**; LOCATE; STORAGE; OUTPUT; QUEUE

Derwent Class: T01

International Patent Class (Main): **G06F-009/46**

International Patent Class (Additional): **G06F-012/16 ; G06F-013/42 ; G06F-015/16**

File Segment: EPI

11/5/33 (Item 26 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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007645884 \*\*Image available\*\*

WPI Acc No: 1988-279816/8840  
XRPX Acc No: N88-212393

**Firmware state machine for data communication system - performs designated operation for line in response to instructions and loads new value corresp. to starting instruction of next state**  
Patent Assignee: BULL HN INFORMATION SYSTEMS INC (HONE ); HONEYWELL BULL INC (HONE )

Inventor: HOLTEY T O; MURRAY T L; PERZAN W A; SMITH S W

Number of Countries: 008 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 285003	A	19881005	EP 88104728	A	19880324	198840 B
AU 8813800	A	19880929				198847
US 4965721	A	19901023	US 8732896	A	19870331	199045
CA 1287932	C	19910820				199138
EP 285003	B1	19940608	EP 88104728	A	19880324	199422
KR 9304949	B1	19930610	KR 883664	A	19880331	199424
DE 3889962	G	19940714	DE 3889962	A	19880324	199428
			EP 88104728	A	19880324	

Priority Applications (No Type Date): US 8732896 A 19870331

Cited Patents: 1.Jnl.Ref; A3...9029; GB 2019697; No-SR.Pub; US 3670306; US 4425616

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 285003	A	F	37		
Designated States (Regional): DE FR GB IT					
EP 285003	B1	E	41	H04Q-003/545	
Designated States (Regional): DE FR GB IT					
DE 3889962	G			H04Q-003/545	Based on patent EP 285003
KR 9304949	B1			G06F-013/10	

Abstract (Basic): EP 285003 A

The state apparatus comprises a processor having a program counter which is employed for control of data transfer. A processor memory is associated with the processor and has a number of firmware **instructions** divided into groups based upon the number of predefined states which are required for performing data transfer. Certain groups of **instructions** include test **instructions** for evaluating conditions related to the line to control sequencing to a next one of the predefined states.

A shared memory has a number of locations for line table information for one line with one **location** containing a program counter **address specifying** a starting **instruction** of a corresponding one of the group of **instructions** to be executed by the processor.

ADVANTAGE - Reduced processor overhead and eliminates problems associated with interrupt driven and polling scheme systems.

1/12

Title Terms: FIRMWARE; STATE; MACHINE; DATA; COMMUNICATE; SYSTEM; PERFORMANCE; **DESIGNATED** ; OPERATE; LINE; RESPOND; **INSTRUCTION** ; LOAD; NEW; VALUE; CORRESPOND; START; **INSTRUCTION** ; STATE

Derwent Class: T01; W01

International Patent Class (Main): **G06F-013/10** ; H04Q-003/545

International Patent Class (Additional): **G06F-003/00** ; **G06F-009/00** ;

**G06F-011/28** ; **G06F-013/12** ; H04Q-003/54

File Segment: EPI

11/5/34 (Item 27 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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007457979 \*\*Image available\*\*

WPI Acc No: 1988-091913/198813

XRPX Acc No: N88-069422

**I-O multi-level communication method for computer system - using shared memory structures in main memory, commonly connected to each processor**

and I-O adaptor in system

Patent Assignee: DATAPOINT CORP (DATA-N)

Inventor: FISCHER M A

Number of Countries: 020 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8802149	A	19880324	WO 87US2394	A	19870918	198813	B
AU 8781576	A	19880407				198827	
US 4783730	A	19881108	US 86910006	A	19860919	198847	
EP 329680	A	19890830	EP 87907171	A	19870918	198935	
CA 1286787	C	19910723				199134	
EP 329680	B1	19931201	EP 87907171	A	19870918	199348	
			WO 87US2394	A	19870918		
DE 3788354	G	19940113	DE 3788354	A	19870918	199403	
			EP 87907171	A	19870918		
			WO 87US2394	A	19870918		

Priority Applications (No Type Date): US 86910006 A 19860919

Cited Patents: US 4253146; US 4415971; US 4426679; US 4644463; 01Jnl.Ref;

EP 49158; US 4402046

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8802149	A	E	81		
				Designated States (National):	AU BR DK FI JP KP NO
				Designated States (Regional):	AT BE CH DE FR GB IT LU NL SE
US 4783730	A		34		
EP 329680	A	E			
				Designated States (Regional):	AT BE CH DE FR GB IT LI LU NL SE
EP 329680	B1	E	48	G06F-013/00	Based on patent WO 8802149
				Designated States (Regional):	AT BE CH DE FR GB IT LI LU NL SE
DE 3788354	G			G06F-013/00	Based on patent EP 329680
					Based on patent WO 8802149

Abstract (Basic): WO 8802149 A

The communication method uses a multi-level communicating structure. The first memory, **designated** a mailbox is established for holding data for communicating module information between each processor and each I/O adapter (22). A second memory holds data for communicating I/o, device information between processors and the I/o devices associated with each adapter. A third memory holds data for communicating I/o device **operations** and for transferring data to and from the I/o device using predetermined memory locations.

A fourth memory is optionally established for holding data for communicating additional I/o device **operations** when the third memory is of insufficient **capacity** to fully **specify** the I/o device **operation**.

ADVANTAGE - Increased data throughput and efficiency.

1/14

Title Terms: I-O; MULTI; LEVEL; COMMUNICATE; METHOD; COMPUTER; SYSTEM; SHARE; MEMORY; STRUCTURE; MAIN; MEMORY; COMMON; CONNECT; PROCESSOR; I-O; ADAPT; SYSTEM

Derwent Class: T01

International Patent Class (Main): **G06F-013/00**

International Patent Class (Additional): **G06F-015/16**

File Segment: EPI

11/5/35 (Item 28 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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004497846

WPI Acc No: 1986-001190/198601

XRPX Acc No: N86-000909

**Input-output computer bus data communication - having interrupt bus connected to each of units of computer system including several processors and CPU**

Patent Assignee: CONVEX COMPUTER CORP (CONV-N)  
Inventor: GANT A D; JONES T M; KIMMEL A T; NOBLES D A  
Number of Countries: 004 Number of Patents: 004  
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 165600	A	19851227	EP 85107568	A	19850619	198601 B
US 4868742	A	19890919	US 88206962	A	19880609	198947
EP 165600	B	19911121				199147
DE 3584690	G	19920102				199202

Priority Applications (No Type Date): US 84622561 A 19840620  
Cited Patents: 5.Jnl.Ref; A3...8831; EP 109308; No-SR.Pub; US 4009470; US 4403282

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 165600	A	E	39		
Designated States (Regional): DE FR GB					
EP 165600	B				
Designated States (Regional): DE FR GB					

Abstract (Basic): EP 165600 A

A peripheral unit e.g. a processor, transfers a data **block** by transferring a header parcel initially which **defines** an **address**, **block length** and type of **function**. This is transmitted to a memory controller which carries out the desired data transfer by sending or receiving sequential data parcels. An interrupt bus connects each of the units of the **computer system** including **several** processors and a CPU. Any one of the units connected to the bus may interrupt any of the other units.

During interruption, an interrupt vector is sent out on a number of interrupt lines. A receiving unit, the interrupt is identified and the appropriate **function** carried out.

ADVANTAGE - Provides high data bandwidth together with flexible **operation**.

0/7

Title Terms: INPUT; OUTPUT; COMPUTER; BUS; DATA; COMMUNICATE; INTERRUPT;  
BUS; CONNECT; UNIT; COMPUTER; SYSTEM; PROCESSOR; CPU  
Derwent Class: T01  
International Patent Class (Additional): G06F-013/36  
File Segment: EPI

HEADER DEFINES  
ADDRESS &  
LENGTH

11/5/36 (Item 29 from file: 350)  
DIALOG(R) File 350:Derwent WPIX  
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002336860

WPI Acc No: 1980-E3304C/198019

**Input-output rate transfer for data storage discs - has weighting of priority of selected data blocks modified by advancing apparent initial location of blocks**

Patent Assignee: SPERRY RAND CORP (SPER )  
Inventor: ALLAN I D; WALBERG P E  
Number of Countries: 001 Number of Patents: 001  
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 4200928	A	19800429				198019 B

Priority Applications (No Type Date): US 78871283 A 19780123

Abstract (Basic): US 4200928 A

The system is for accessing data **blocks** in a **computer system** having **multiple** -disc drive rotational position sensing which is not centrally synchronised and where data read and write requests are normally weighted by the order of availability of requested data **blocks**. The weighting of the priority, or queue position, of selected data **blocks** is modified by advancing the apparent initial **location**



of data **blocks** designated for preferential access and maintaining an availability signal, or peripheral interrupt, for an extended period.

A special pre-data-transfer **instruction** indicates the duration of the peripheral interrupt. A circuit for implementing the system has a storage register for receiving the special **instruction**, a down counter for decrementing for the duration of the designed pre-data-interrupt and an interrupt duration control latch for issuing and extinguishing the interrupt.

Title Terms: INPUT; OUTPUT; RATE; TRANSFER; DATA; STORAGE; DISC; WEIGHT; PRIORITY; SELECT; DATA; **BLOCK**; MODIFIED; ADVANCE; APPARENT; INITIAL; LOCATE; **BLOCK**

Derwent Class: T01

International Patent Class (Additional): **G06F-013/04**

File Segment: EPI

Set	Items	Description
S1	10423235	INSTRUCTION? OR STATEMENT? OR OPERATION? OR FUNCTION? OR EXECUTION? OR COMMAND?
S2	10292667	DEFINE? OR DEFINING OR SPECIF? OR DESCRIB? OR STIPULAT? OR DESIGNAT?
S3	3062340	ADDRESS? OR LOCATION OR LINK? ? OR URL OR URLS OR (UNIFORM OR UNIVERSAL) ()RESOURCE()LOCATOR? OR NAMESPACE OR DOMAIN
S4	97190	DATA (2N) (ELEMENT? OR VALUE? OR ATTRIBUTE? OR TRAIT? OR FEATURE?)
S5	10851740	LENGTH OR SIZE? OR SIZING OR CAPACITY? OR LIMIT? OR EXTENT OR BOUNDAR? OR THRESHOLD OR STREAM? OR BLOCK?
S6	27213	(MULTIPLE OR MANY OR PLURAL? OR NUMEROUS OR SEVERAL OR DUPLICAT) (2N) (PLATFORM? OR (COMPUTER? OR OPERATING) ()SYSTEM?)
S7	5165	S1 (S) S6
S8	2496964	S2 (S) (S3 OR S4 OR S5)
S9	446635	S2 (5N) (S3 OR S4 OR S5)
S10	91	S7 (S) S8 (S) S9
S11	4	S1 (S) S2 (S) S3 (S) S4 (S) S5 (S) S6
S12	94	S10 OR S11
S13	82	S12 NOT PY>2000
S14	74	S13 NOT PD>20001129
S15	63	RD (unique items)
File	2:INSPEC 1969-2003/Nov W5	(c) 2003 Institution of Electrical Engineers
File	6:NTIS 1964-2003/Dec W1	(c) 2003 NTIS, Intl Cpyrght All Rights Res
File	8:Ei Compendex(R) 1970-2003/Nov W5	(c) 2003 Elsevier Eng. Info. Inc.
File	34:SciSearch(R) Cited Ref Sci 1990-2003/Nov W5	(c) 2003 Inst for Sci Info
File	35:Dissertation Abs Online 1861-2003/Oct	(c) 2003 ProQuest Info&Learning
File	65:Inside Conferences 1993-2003/Dec W1	(c) 2003 BLDSC all rts. reserv.
File	92:IHS Intl.Stds.& Specs. 1999/Nov	(c) 1999 Information Handling Services
File	94:JICST-EPlus 1985-2003/Dec W1	(c)2003 Japan Science and Tech Corp(JST)
File	95:TEME-Technology & Management 1989-2003/Nov W4	(c) 2003 FIZ TECHNIK
File	99:Wilson Appl. Sci & Tech Abs 1983-2003/Oct	(c) 2003 The HW Wilson Co.
File	103:Energy SciTec 1974-2003/Nov B2	(c) 2003 Contains copyrighted material
File	144:Pascal 1973-2003/Nov W5	(c) 2003 INIST/CNRS
File	202:Info. Sci. & Tech. Abs. 1966-2003/Nov 17	(c) 2003 EBSCO Publishing
File	233:Internet & Personal Comp. Abs. 1981-2003/Jul	(c) 2003, EBSCO Pub.
File	239:Mathsci 1940-2003/Jan	(c) 2003 American Mathematical Society
File	275:Gale Group Computer DB(TM) 1983-2003/Dec 08	(c) 2003 The Gale Group
File	434:SciSearch(R) Cited Ref Sci 1974-1989/Dec	(c) 1998 Inst for Sci Info
File	647:CMP Computer Fulltext 1988-2003/Dec W1	(c) 2003 CMP Media, LLC
File	674:Computer News Fulltext 1989-2003/Dec W1	(c) 2003 IDG Communications
File	696:DIALOG Telecom. Newsletters 1995-2003/Dec 08	(c) 2003 The Dialog Corp.

15/5/10 (Item 10 file: 2)

DIALOG(R) File 2:INSPEC

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5130752 INSPEC Abstract Number: C9601-7840-051

**Title: Using an instruction interpreter to link the GIS database to multiple DBMS**

Author(s): Crichton, W.

Author Affiliation: Facility Mapping Syst. Inc., Mill Valley, CA, USA

Conference Title: GIS/LIS Proceedings Part vol.1 p.140-6 vol.1

Publisher: American Soc. Photogrammetry & Remote Sensing & American Congress on Surveying & Mapping, Bethesda, MD, USA

Publication Date: 1993 Country of Publication: USA 2 vol.xiii+835 pp.

ISBN: 0 944426 99 9

Conference Title: Proceedings of Geographic Information Systems/Land Information Systems Convention (GIS/LIS)

Conference Sponsor: American Congress on Surveying & Mapping; American Soc. Photogrammetry & Remote Sensing; AM/FM Int.; et al

Conference Date: 2-4 Nov. 1993 Conference Location: Minneapolis, MN, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: Communications between geographic information systems and multiple databases are a growing problem. With the number of available product options, file formats, and data storage choices increasing, confusion will most likely grow before industry wide standards emerge. This situation leaves little choice to GIS software developers/project managers: do nothing or invest heavily in expensive individual interfaces. However, new products recently introduced are proving to be an immediate, low risk way to side step this problem. As the GIS database matures, there is constant pressure to "link" it to multiple commercial DBMS within the departmental and/or enterprise information system. The conventional solution is to implement site/product **specific** interfaces. Such single customer **links** often prove to be uneconomical quality assurance nightmares. A new approach makes it possible for a single GIS user interface to transmit "logic calls" to a commercially offered ("black box") interpreter. These requests are in turn transformed into **instructions** that can be understood by a variety of DBMS products operating on **multiple** hardware/OS **platforms**. A single interface investment therefore makes it possible to interactively **link** the GIS to many different DBMS/data formats. This "**command** interpretation" approach offers an economic solution today, rather than waiting for universal standards to mitigate this tomorrow. (0 Refs)

Subfile: C

Descriptors: distributed databases; geographic information systems; program interpreters; user interfaces; visual databases

Identifiers: instruction interpreter; GIS database; multiple DBMS; geographic information systems; multiple databases; product options; file formats; data storage choices; industry wide standards; GIS software developers/project managers; multiple commercial DBMS; site/product specific interfaces; single customer links; uneconomical quality assurance; GIS user interface; logic calls; black box interpreter; DBMS products; multiple hardware/OS platforms; interface investment; DBMS/data formats; command interpretation

Class Codes: C7840 (Geography and cartography computing); C6160S (Spatial and pictorial databases); C6160B (Distributed databases); C6180 (User interfaces); C6150C (Compilers, interpreters and other processors)

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COMMANDS

15/5/20 (Item 1 from File: 8)  
DIALOG(R) File 8: Ei Compendex(R)  
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05125332 E.I. No: EIP98094392236

**Title: Open systems: Reality or illusion?**

Author: Warrior, Jay

Source: Sensors (Peterborough, NH) v 15 n 9 pt 1 Sep 1998. 4p

Publication Year: 1998

CODEN: SNSRES ISSN: 0746-9462

Language: English

Document Type: JA; (Journal Article) Treatment: G; (General Review); T; (Theoretical)

Journal Announcement: 9811W4

Abstract: An open system provides capabilities that enable properly implemented applications to run a variety of **platforms** from **multiple** vendors; is interoperable with other systems applications; and presents a consistent style of interaction with the user. This system must be consensus driven and standard based and have **specifications** that are freely available at low cost to any interested parties. The **domain** of a system is **defined** by the set of components and the types of **functions** the system **addresses**. The components and **functions** help identify the problem **addressed** by the system. The components **define** the magnitude of the system, and the **functions** provide the scope of complexity.

Descriptors: \*Open systems; Computer systems programming; Computer networks; Network protocols; Computer simulation languages; Computer architecture; Interconnection networks; Artificial intelligence; Formal logic; Response time (computer systems)

Identifiers: Open system interconnection (OSI); Unified modeling languages

Classification Codes:

723.1.1 (Computer Programming Languages)

723.1 (Computer Programming); 703.1 (Electric Networks); 723.4 (Artificial Intelligence)

722 (Computer Hardware); 723 (Computer Software); 703 (Electric Circuits)

72 (COMPUTERS & DATA PROCESSING); 70 (ELECTRICAL ENGINEERING)

15/5/22 (Item 3 from File: 8)  
DIALOG(R)File 8:Ei Compendex(R)  
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03013344 E.I. Monthly No: EIM9101-003344

**Title: ECL RISC microprocessor designed for two level cache.**

Author: Roberts, David; Layman, Tim; Taylor, George

Corporate Source: MIPS Computer Systems, Inc, Sunnyvale, CA, USA

Conference Title: Digest of Papers - Thirty-Fifth IEEE Computer Society  
International Conference - COMPCON Spring '90

Conference Date: 19900226

Sponsor: IEEE Computer Soc

E.I. Conference No.: 13939

Source: Dig of Pap Thirty Fifth IEEE Comput Soc Int Conf COMPCON 89. Publ  
by IEEE, IEEE Service Center, Piscataway, NJ, USA (IEEE cat n 90CH2843-1).  
p 228-231

Publication Year: 1990

ISBN: 0-8186-2028-5

Language: English

Document Type: PA; (Conference Paper) Treatment: T; (Theoretical); A;  
(Applications)

Journal Announcement: 9101

Abstract: Reduced- **instruction** -set-computer (RISC) architectures, by  
virtue of their **streamlined instruction** set and more efficient use of  
fundamental machine resources, are capable of exploiting emerging VLSI  
technologies more quickly than traditional, more complicated machine  
architectures. Bipolar emitter-coupled-logic (ECL) technology offers  
shorter propagation delays and higher toggle rates than other circuit  
technologies. This, coupled with its ability to drive transmission lines  
and large capacitive loads, has made ECL the technology of choice for **many**  
high-speed **computer systems**. The lower circuit density and high-power  
requirements of traditional ECL have prevented its use in low-cost  
microprocessor-based system designs. Recent advances in density and power  
consumption of VLSI ECL technology have widened the technology envelope to  
the point at which it has become an attractive target for RISC processor  
designs. The four VLSI chips **described** provide **address** translation, the  
control logic for a two-level cache, and a system bus interface in addition  
to the basic integer and floating-point data paths. The chip set consists  
of the R6000 CPU, the R6010 floating-point controller, the BIT B3110  
floating-point multiply/divide unit, and the R6020 system bus controller. 7  
Refs.

Descriptors: \*COMPUTER ARCHITECTURE--\*Reduced Instruction Set Computing;  
LOGIC CIRCUITS, EMITTER COUPLED; INTEGRATED CIRCUITS, VLSI

Identifiers: TWO-LEVEL CACHE; RISC MICROPROCESSOR; STREAMLINED  
INSTRUCTION; TOGGLE RATES; VLSI ECL; HIGH-SPEED COMPUTER

Classification Codes:

722 (Computer Hardware); 723 (Computer Software); 721 (Computer  
Circuits & Logic Elements); 713 (Electronic Circuits); 714 (Electronic  
Components)

72 (COMPUTERS & DATA PROCESSING); 71. (ELECTRONICS & COMMUNICATIONS)

15/3,K/51 (Item 4 from file: 647)  
DIALOG(R) File 647: CMP Computer Fulltext  
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01023782 CMP ACCESSION NUMBER: NWC19940404S3539  
**Netware 4.x tape backup nlms** (Previously Reviewed)  
NETWORK COMPUTING, 1994, n 504, 119  
PUBLICATION DATE: 940404  
JOURNAL CODE: NWC LANGUAGE: English  
RECORD TYPE: Fulltext  
SECTION HEADING: Reviews

TEXT:

... 110. Circle reader service 441. ARCserve Cheyenne Software Wins the -number of agents- contest, supporting Mac and **multiple** Unix client **platforms**. Superior file and tape management **functionality** and multitasking are key benefits. It does not fully support SMS. March 1, 1994, page 110. Circle...

...tape rotation algorithms. March 1, 1994, page 110. Circle reader service 443. NetWorker Legato Systems Continues to **define** -state of the art- in NLM -based network backup, taking performance honors. March 1, 1994, page 110...

...Apple's PowerBook utilities. Unable to identify a change in a file on both sides of a **link**. March 1, 1994, page 140. Circle reader service 450. CPU-EASYSYNC v2.01 Connectix A different approach to synchronization, intercepting Finder copy **commands**. March 1, 1994, page 140. Circle reader service 451. Magnet v1.01 No Hands Software Problems dealing...

...140. Circle reader service / headline 452. Norton Essentials PowerBook Symantec Corp. Advanced features, but does not modify **links** once **defined**. March 1, 1994, page 140. Circle reader service 453. FileRunner v1.0 MBS Technologies Not many added features; lets you modify **defined links**. March 1, 1994, page 140. Circle reader service 454. Inline Sync v1.0.1 Inline Software The...

...reader service 455. UpToDate v1.3 Ben Heckster's Features such as a database to track file **location** make this product stand out. It's free. March 1, 1994, page 140. Circle reader service 456...

15/3,K/52 (Item 5 from file: 647)  
DIALOG(R) File 647: CMP Computer Fulltext  
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00605911 CMP ACCESSION NUMBER: NWC19911001S1310  
**Lotus Notes and DDE: Strangers on a Train?** (Environments)  
Stephen Morse  
NETWORK COMPUTING, 1991, n 210, 12  
PUBLICATION DATE: 911001  
JOURNAL CODE: NWC LANGUAGE: English  
RECORD TYPE: Fulltext  
SECTION HEADING: Logging On

TEXT:

... they've decided that Notes is the only application they will buy and run on their Windows **platforms**. But **many** other organizations have discovered that no one application...

...Wouldn't it be nice, for example, to be able to ask Notes for the complete inside **address** when you're using Word for Windows or Ami to create a business letter? Names, **addresses** and other business-related information are the kinds of things that Notes is supposed to be good...

...What about Notes as a DDE client? It's certainly very easy to set up a hot **link** between Notes and another application, say Ami. You merely

highlight the section in the other application that...

...linked, copy it to the Clipboard, and then in Notes, do a Paste Special with the hot- **link** option enabled. No rocket science involved here. But see what happens when you or another user returns to view the Notes document that contains the hot **link**. If Notes behaved like other DDE-aware applications, we'd expect that as soon as you opened the document in question, you'd be asked automatically whether you wanted to re-establish the hot **link**. You wouldn't have to know in advance or remember that such a **link** existed. But Notes offers no such reminder. You have to remember to double-click on the hot...

...a user to remember these things? What about users who don't understand things such as hot **links**, those who expect (and rightly so) that the application will have enough intelligence to handle these things? There is another point about Notes hot **links**: How do you know they're there? When you first open a document with a hot **link** in it, the section with the hot **link** looks like any other part of the document. If you turn on Enable Edit (assuming you have the access right to do so), you can see that the part containing the hot **link** has double half-brackets (but you'd better look carefully). If you don't have edit access...user has been sheltered from (and has, for the most part, had only externally controlled and externally **limited** access to) the raw data by the application's actions. In the Real World Now consider production...

...thing to look for is the set of fields (or columns, to use the relational term) that **define** a record. In the ideal world of demos and marketing presentations, these columns are always called something...brnst in the data dictionary, usually you find a simple **statement** that tells you informative things, such as the field is a character field, it's 36 characters...B" or "\*" or "7" or any other character. If you check the data dictionary, you'll find **specifications** like "Character Field" and "Width 1," and sometimes "Must contain 1, 2 or T." 1, 2 or...

...longer clear. Often these flags which are usually used in combination with other flags or with certain **data value** ranges...information that users require once a product is installed and configured. Such documentation should be organized into **functional** categories, allowing users to locate needed information quickly. For important product features such as **function** key layout, many vendors include card-based references that save users from having to thumb through manuals...

...tutorials and references. A well structured table of contents is a must. The manual should include a **statement** of its intended use and audience, including a description of what the user should know before installing...

...is one that has been carefully thought out and constructed. For example, don't simply list a **function** under its standard name. Try to think of every possible way that a user might locate information for a particular **function**. To improve a user's ability to learn or locate information, some vendors provide disk-based documentation...

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**Web application servers power e-commerce  
Roundup looks at eight leading products.**

Byline: By Paul Ferrill

Journal: Network World Page Number: 108

Publication Date: September 25, 2000

Word Count: 2955 Line Count: 286

**Text:**

... an object-oriented framework for creating server-side applications. These applications run inside a container, or separate **execution** space, in the application server. The EJB 2.0 **specification** was released in draft form at the JavaOne 2000 conference in May. The products in this review support the EJB 1.1 final **specification**. The Java 2 Enterprise Edition (J2EE) **specification** encompasses a number of **functional** areas that **define** the components needed to implement robust e-commerce solutions. Version 1.3, released in draft form in August, is the most recent release of the J2EE **specification**. Most of the products in this review comply with J2EE 1.2 (See graphic, page 114).For...

... Key features that stress ease of use include prebuilt tag libraries of common Java Server Pages (JSP) **functions** and a browser-based JRun Management Console (JMC). An integrated development environment named JRun Studio, targeted at...

... 3.0. JRun Server comes in three editions: Enterprise, Professional and Developer. The Developer Edition is a **limited** version (three concurrent connections, no clustering support) of the Enterprise Edition, available free for download from its...

... targeted at developers, supports JSP and Java servlet development. The Enterprise Edition includes support for all EJB **functionality**, including Java Message Service (JMS), Java Transaction API (JTA) and clustering. Installing JRun Server was simple, straightforward...

... appropriate values and by verifying that key EJB required classes are compliant with the EJB 1.1 **specification**. A graphical utility called the WebLogic Zero Administration Client (ZAC) Publish Wizard lets you create, publish and...

... player in the high-end application server market. The product, previously known as Sapphire/Web, combines the **functionality** from earlier versions and adds support for the J2EE standards. Bluestone provides a J2EE Developer program that... is an XML development environment included with UBS that makes it possible to browse databases and ObindO **data elements** to XML, DTD and Document Object Model trees. Visual-XML is written in pure Java, meaning it...

... XML (1.3) includes a number of wizards to walk you through the process of creating JavaBeans, **specifying** XML output characteristics and **defining** filters based on bean methods. Bluestone has gone to great lengths to position its product as a...

... Visual-XML and the J2EE Developer, Bluestone has taken great strides on the usability front, with added **functionality** that its competitors charge extra for. IBM WebSphere 3.5 IBM is trying to regain the position of...

... started building and deploying enterprise applications. The Graphical Application Builder is an assembly tool that lets you **link** EJB components to create an application. IAS does not come with any tools for developing applications. Writing...

... its Web site ([www.iona-portal.com/suite/apcontact.htm](http://www.iona-portal.com/suite/apcontact.htm)). The current



version of iAS lacks the **functionality** found in most of the other products we evaluated. From a purely ease-of-use perspective, youOre...  
...the product it sells. IAS 6.0, released in May, meets the requirements of the latest J2EE **specification** and has passed the full J2EE Certification Test Suite. Basic core services of iAS include a transaction...unique position with respect to installed customer base. OracleOs database product is unquestionably the market leader on **multiple platforms**. OracleOs Internet Application Server (iAS) has a unique advantage in that it is intertwined with the rest...

... can be deployed as servlets, JSPs, EJBs or CORBA objects. An XML developerOs kit contains basic building **blocks** for reading, interpreting and viewing XML documents. None of the Oracle iAS distributions include Java development tools...

... can put their Oracle Forms and Oracle Reports to work on the Web with little effort. This **functionality** comes with a hefty price tag. Oracle iAS was the most expensive product in this roundup. SilverStream...

... the SilverStream Application Server parameters takes place using the SilverStream Management Console. SilverStream Designer is a full- **function** design environment for building complete Web applications, including those that generate HTML for viewing as Web pages...

... syntax, lists of available objects and methods and a special toolbox with buttons that add code to **define specific functions**. A fully **functional** 45-day trial version of SilverStreamOs product includes a complete tutorial and extensive help and can be...a list of requirements for the task should help in the decision process. The list should include **specific** information like expected traffic for the site, legacy application connectivity requirements, database requirements and deployment schedule. Once...

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# **Unplugging the LAN**

**The first batch of products to support the IEEE 802.11 wireless Ethernet standard shows promise, not perfection.**

Byline: Christopher Null

Journal: Network World Page Number: 43

Publication Date: February 08, 1999

Word Count: 1926 Line Count: 178

## **Text:**

... 500 feet or more - but don't believe everything you hear. The 802.11 standard is the **specification** for spread spectrum wireless LAN technologies using multiple channels along the 2.4-GHz band. Its use...

... environment also likely explains why performance, even at 32 feet, is substantially off the 2M bit/sec **specification**. Surfing another kind of waveNortel's BayStack 660 package has an interesting genealogy. It started out as...

... 2 interfaces. The Java-based setup and configuration utility for the access point is glacially slow but **functionally** complete. Once you launch the configuration utility, it traps the access point's periodic BOOTP requests and lets you assign a new IP **address** to the unit. Other advanced configuration options are probably not necessary for most users. The access point...

... setup and management of the PC Card clients are exceptionally good. Installing drivers and assigning an IP **address** to a card is a snap, and the extra utilities (especially the detailed Site Survey utility, for...

... neat security feature that lets you allow and deny access on a card-by-card basis, by **designating** media access control (MAC) **addresses**. Nortel's manuals are fair, often showing you screen shots of dialog boxes but not explaining what... organized documentation and driver updates. Of special note with the WaveLAN product is its broad support for **numerous operating systems**, including MacOS. You can also add a second PC Card to the access point for extra bandwidth...

... the RoamAbout PC Card is clearly an OEM version of Lucent's WaveLAN. The two PC Cards **function** identically and even work with each other's drivers. They also use the same client management software...

... bit/sec at 70 feet. Range topped out at 75 feet. How does Aironet's wireless card **command** roughly twice the performance of its competitors? The trick is in a proprietary transfer protocol layered on...

... or HTTP session. We thought Aironet's client-based software also needed major work to enhance its **functionality** and usability, but overall, the management tools got the job done. Installing the PC4800 PC Card in...

...s PC Card will work with 802.11 access points and vice versa; of course, they are **limited** to 802.11 throughput, which we clocked at an average of 1.28M bit/sec at 32...